

CLASSIC

Modelling, Specification, and Verification

using UPPAAL

Kim Guldstrand Larsen



BRICS
Basic Research
in Computer Science



CENTER FOR INDLEJREDE SOFTWARE SYSTEMER

Modelling using Finite State Machines



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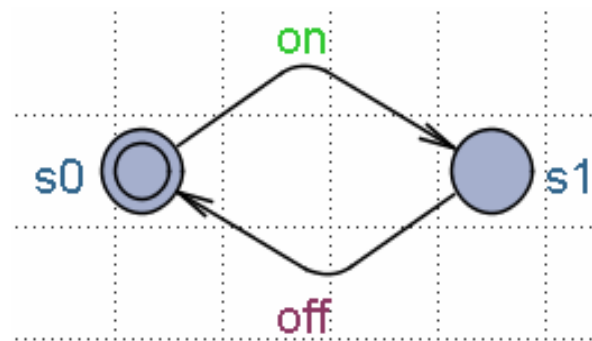


Modelling processes

- ❖ A process is the execution of a sequential program.
- ❖ modeled as a finite state machine (LTS)
 - transits from state to state
 - by executing a sequence of *atomic* actions.

a light switch

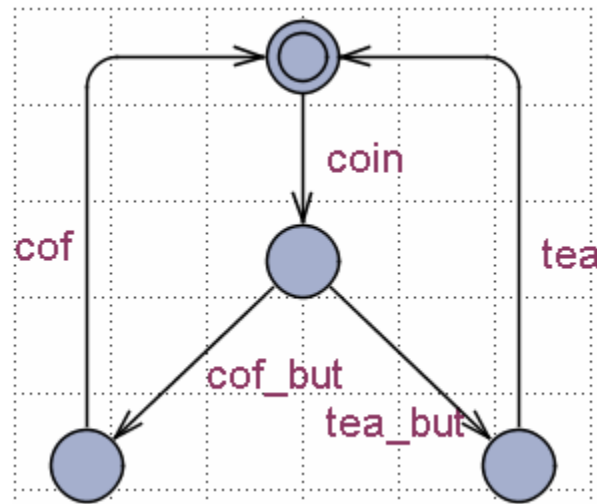
LTS



on → off → on → off → on → off →

a sequence of
actions or *trace*

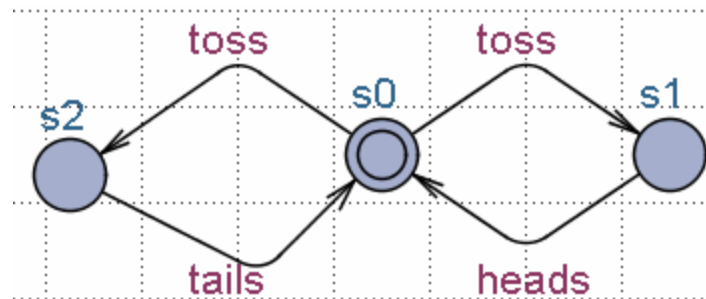
Modelling Choices



- Who or what makes the choice?
- Is there a difference between input and output actions?

Non-deterministic Choice

❖ Tossing a coin



❖ Possible traces?

- Both outcomes possible
- Nothing said about relative frequency
- If coin is fair, the outcome is 50/50

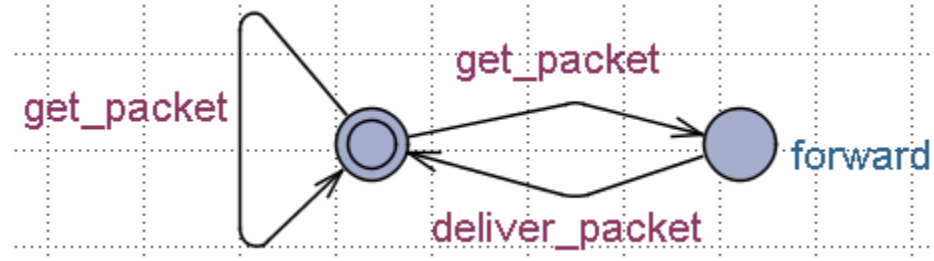
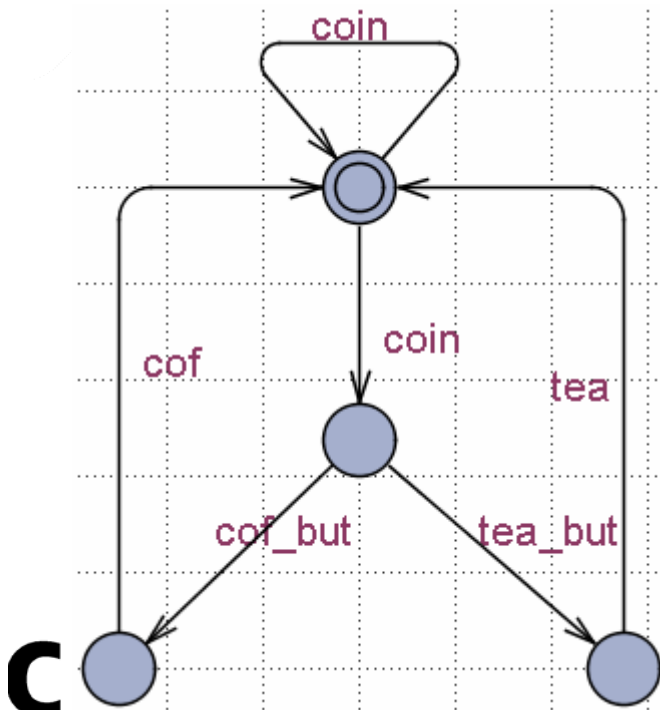
Non-Deterministic Choice modelling failure



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How do we model an unreliable communication channel which accepts **packets**, and if a failure occurs produces no output, otherwise **delivers** the packet to the receiver?

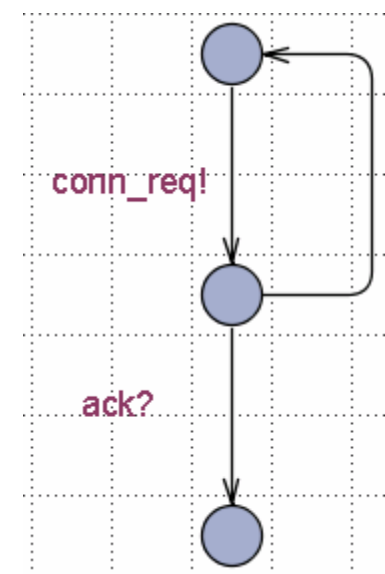
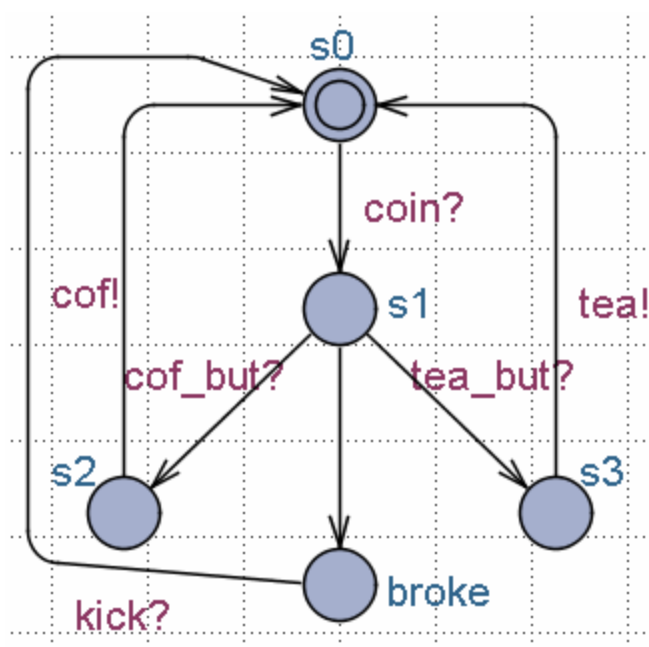
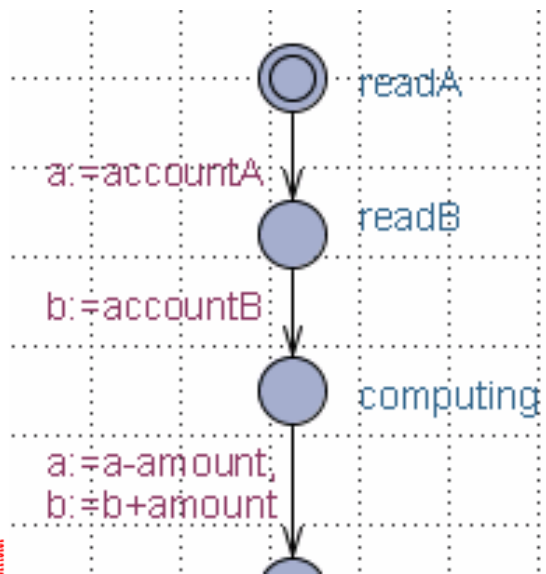
Use non-determinism...



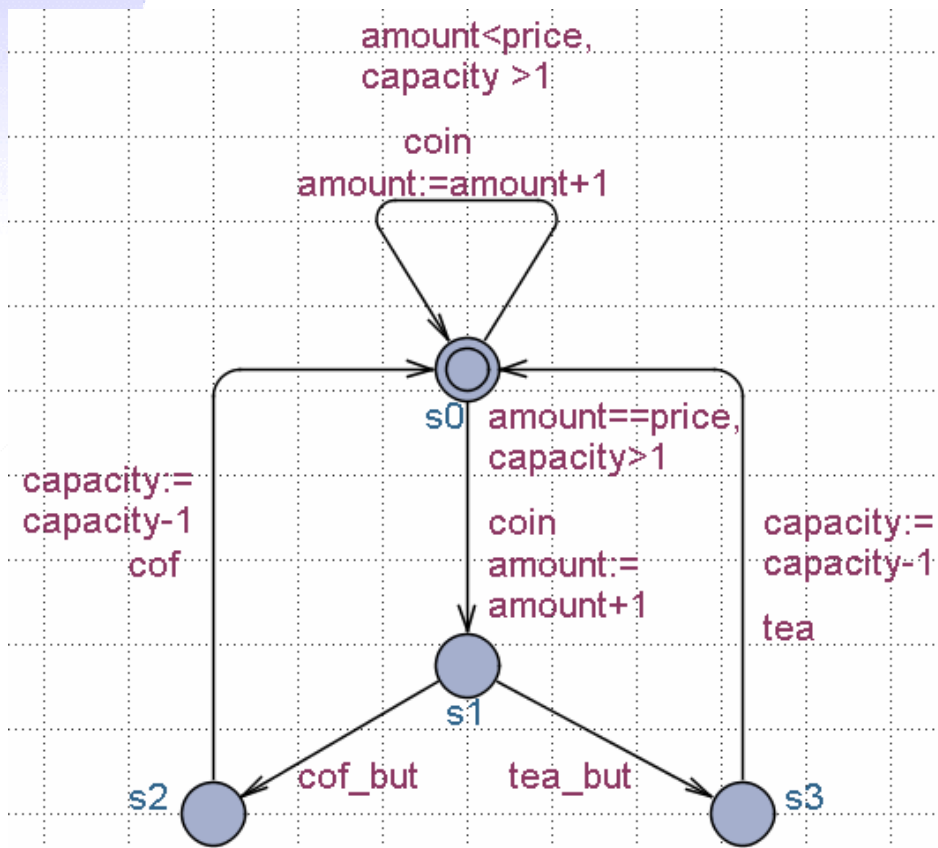


Internal-Actions

- ❖ Spontaneous actions
- ❖ Internal actions
- ❖ Tau-actions
- ❖ Internal transitions can be taken on the initiative of a single machine without communication with others



Extended FSM



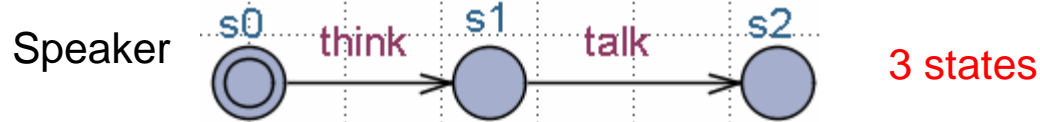
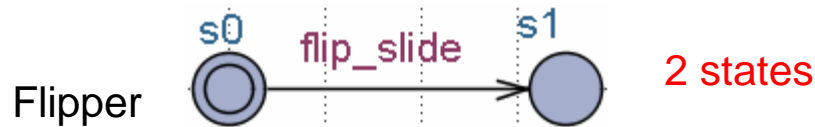
- **EFSM** =
FSM +
variables +
enabling conditions +
assignments
- Transition still atomic
- Can be translated into FSM if variables have bounded domain
- State: **control location**
+ **variable values**:

(**state**, **amount**, **capacity**)
- (**s0**, **5**, **10**)

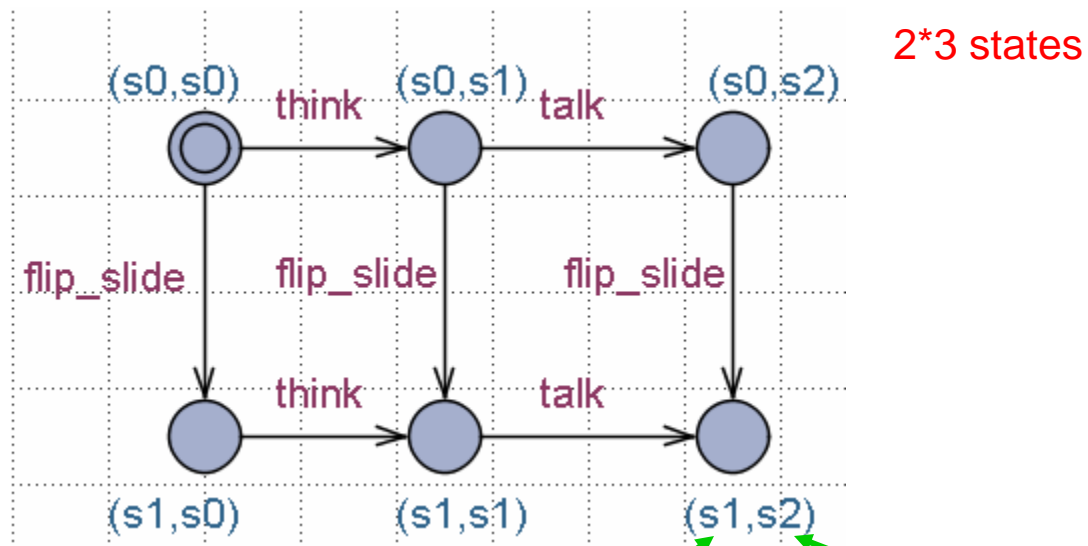
Parallel Composition: interleaving



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Lecturer =
Speaker || Flipper



from Flipper
Kim G. Larsen

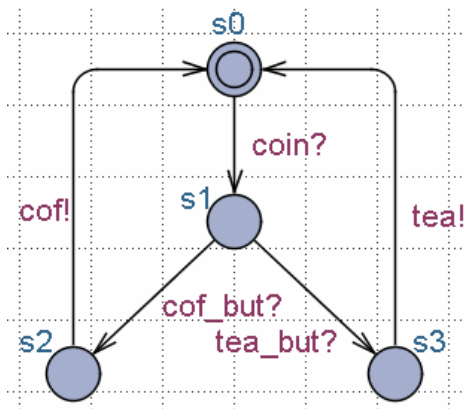
from Speaker



Process Interaction

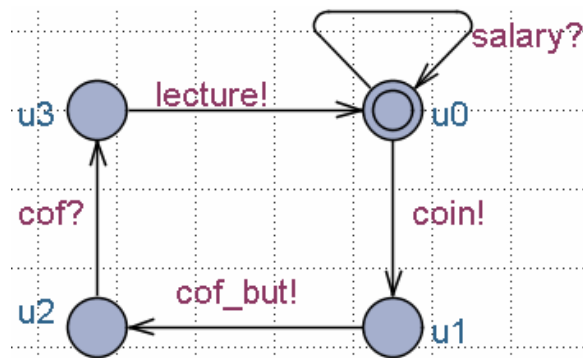
- ❖ ! = Output, ? = Input
- ❖ Handshake communication
- ❖ Two-way

Coffee Machine



4 states

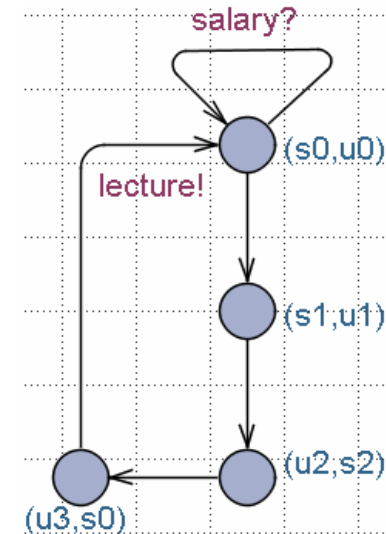
Lecturer



4 states

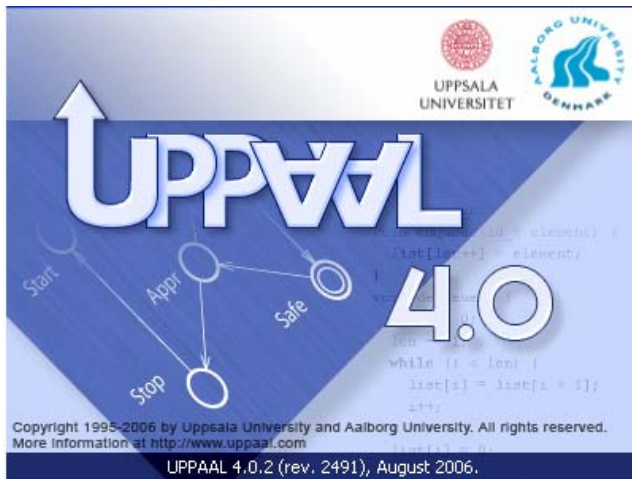
University =
Coffee Machine || Lecturer

- LTS?
- How many states?
- Traces ?



synchronization results in internal actions

4 states: Interaction constrain overall behavior



Adding Time



Collaborators

@UPPsala

- Wang Yi
- Paul Pettersson
- John Håkansson
- Anders Hessel
- Pavel Krcal
- Leonid Mokrushin
- Shi Xiaochun



@AALborg

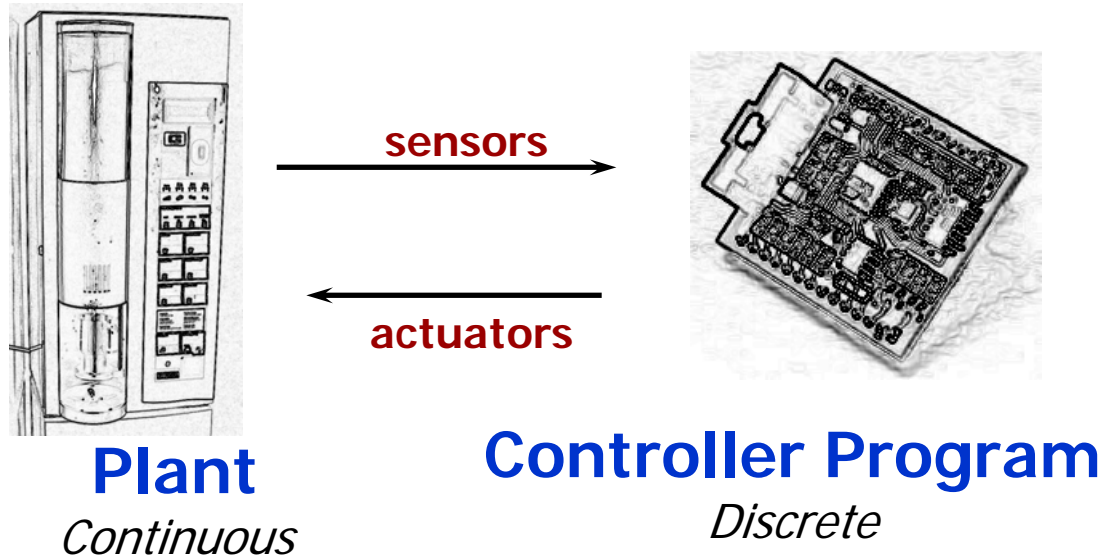
- Kim G Larsen
- Gerd Behrman
- Arne Skou
- Brian Nielsen
- Alexandre David
- Jacob I. Rasmussen
- Marius Mikucionis
- Thomas Chatain



@Elsewhere

- Emmanuel Fleury, Didier Lime, Johan Bengtsson, Fredrik Larsson, Kåre J Kristoffersen, Tobias Amnell, Thomas Hune, Oliver Möller, Elena Fersman, Carsten Weise, David Griffioen, Ansgar Fehnker, Frits Vandraager, Theo Ruys, Pedro D'Argenio, J-P Katoen, Jan Tretmans, Judi Romijn, Ed Brinksma, Martijn Hendriks, Klaus Havelund, Franck Cassez, Magnus Lindahl, Francois Laroussinie, Patricia Bouyer, Augusto Burgueno, H. Bowmann, D. Latella, M. Massink, G. Faconti, Kristina Lundqvist, Lars Asplund, Justin Pearson...

Real Time Systems



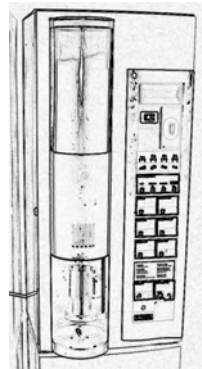
Eg.: Realtime Protocols
Pump Control
Air Bags
Robots
Cruise Control
ABS
CD Players
Production Lines

Real Time System

A system where correctness not only depends on the logical order of events but also on their **timing!!**

Real Time Model Checking

Plant
Continuous



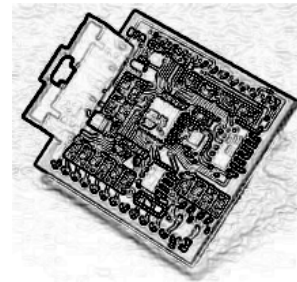
sensors



actuators



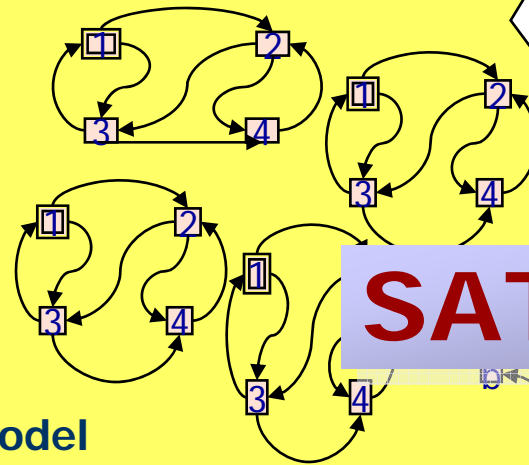
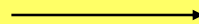
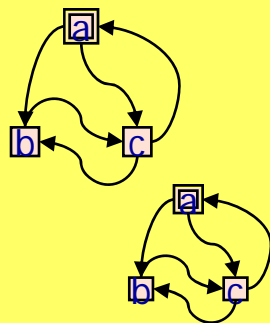
Controller Program
Discrete



Model of tasks (automatic?)



Model of environment (user-supplied / non-determinism)

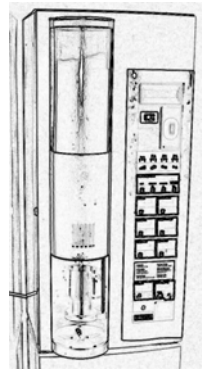


UPPAAL Model

SAT ϕ ??

Real Time Control Synthesis

Plant
Continuous



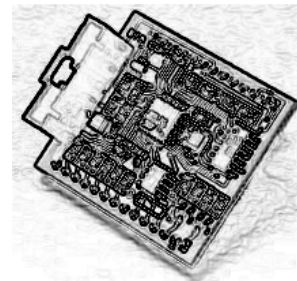
sensors



actuators



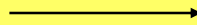
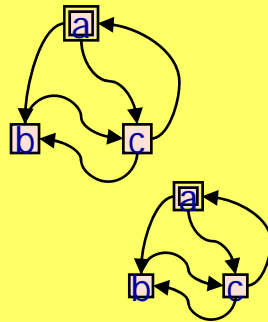
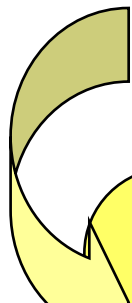
Controller Program
Discrete



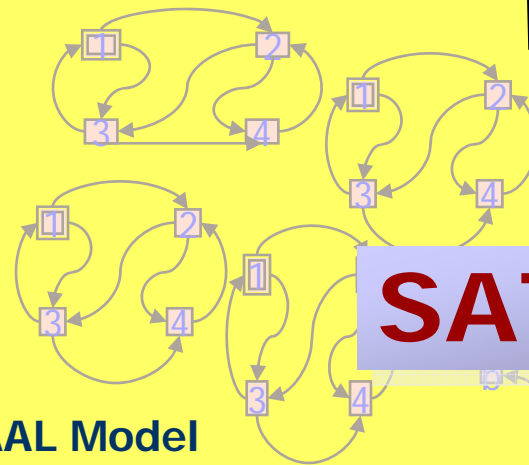
Synthesis
of
tasks/scheduler
(automatic)



Model
of
environment
(user-supplied)

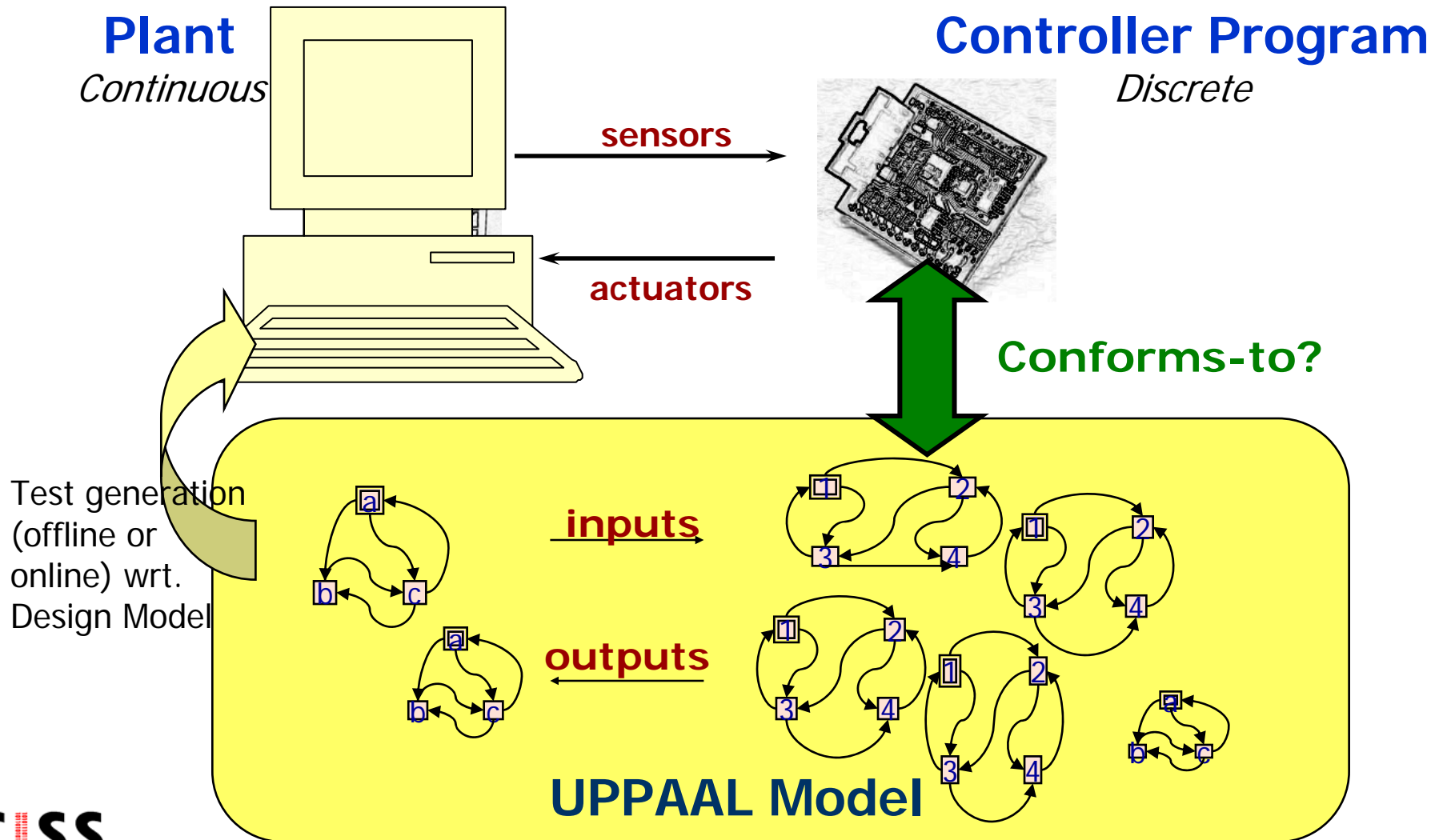


Partial UPPAAL Model



SAT ϕ !!

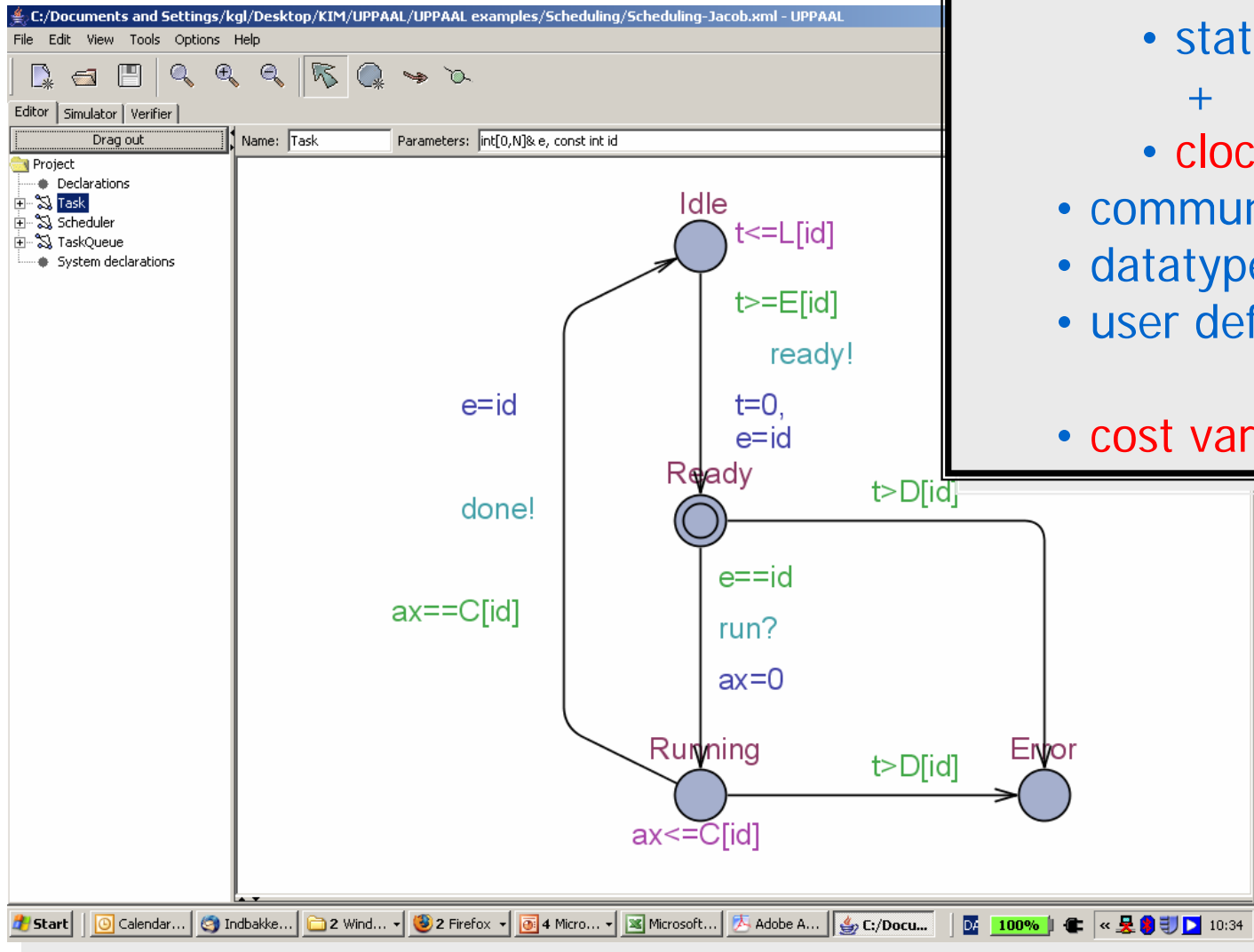
Real-time Model-Based Testing



UPPAAL

Graphical Design Tool

- timed automata =
 - state machines
 - +
 - **clocks**
- communication
- datatypes
- user defined functions
- **cost variable**



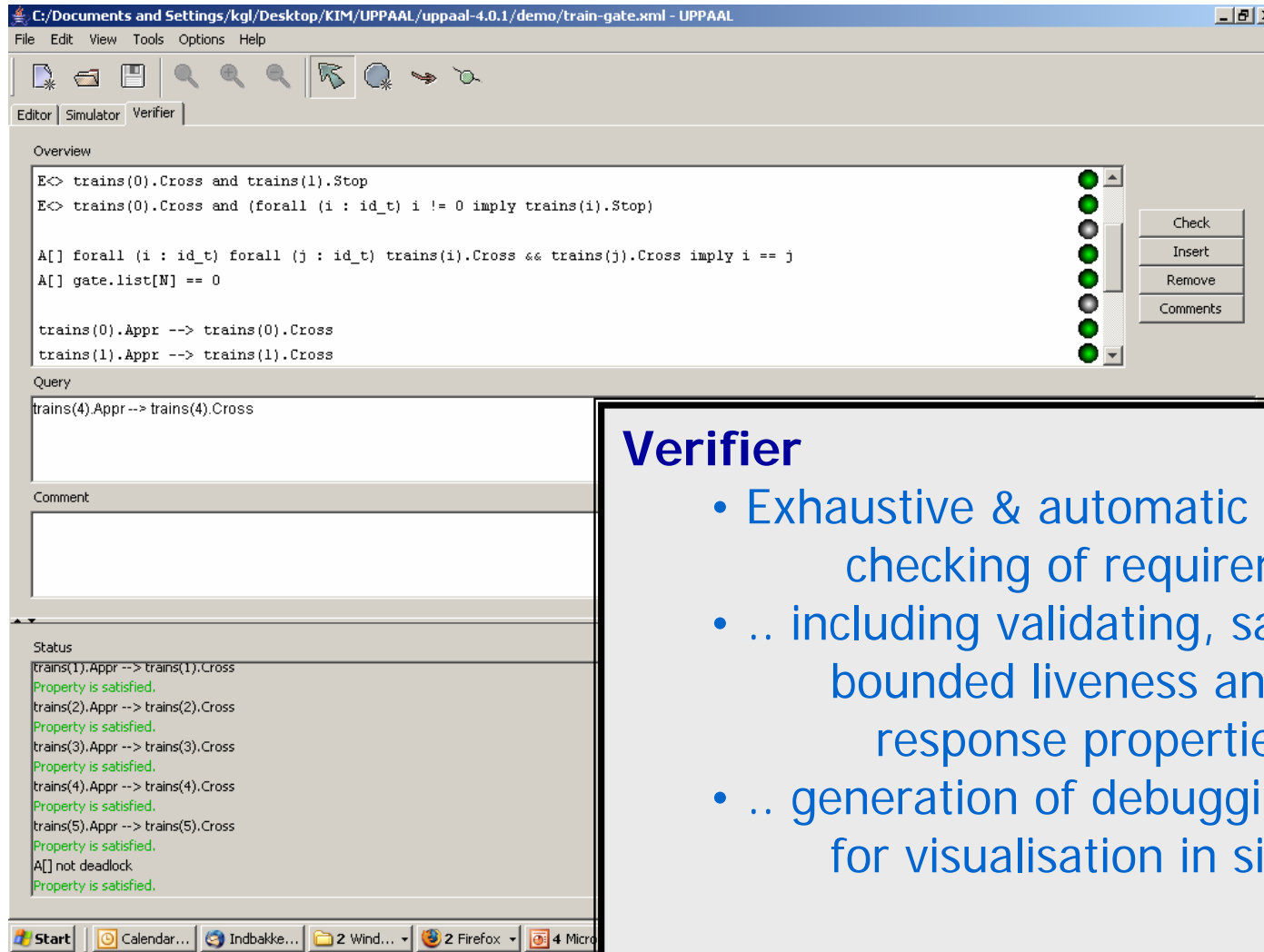
UPPAAL

Graphical Simulator

- visualization and recording
- inexpensive fault detection
- inspection of error traces
- Message Sequence Charts
- (Gantt Charts)

The screenshot displays the UPPAAL graphical simulator interface. The main window shows three task state machines (Task0, Task1, Task2) and a Scheduler. Task0 and Task1 are in the 'Idle' state, while Task2 is also in 'Idle'. The Scheduler is in the 'Free' state. The simulation trace on the left shows the sequence of events: (Ready, Idle, Idle, Free, Shiftdown), Queue, (Ready, Idle, Idle, Free, Start), nonempty: Queue --> Scheduler, (Ready, Idle, Idle, Select, Start), hd: Scheduler --> Queue, (Ready, Idle, Idle, -, Start), run: Scheduler --> Task0, (Running, Idle, Idle, Occ, Start), done: Task0 --> Scheduler, (Idle, Idle, Idle, -, Start), rem: Scheduler --> Queue. The variables window on the right shows the current state of the system: el = 2, E[0] = 20, E[1] = 20, E[2] = 10, L[0] = 30, L[1] = 25, L[2] = 12, D[0] = 30, D[1] = 25, D[2] = 12, C[0] = 4, C[1] = 2, C[2] = 1, P[0] = 1, P[1] = 2, P[2] = 3, Queue.list[0] = 2. The bottom status bar shows the system tray with various icons and the time 10:37.

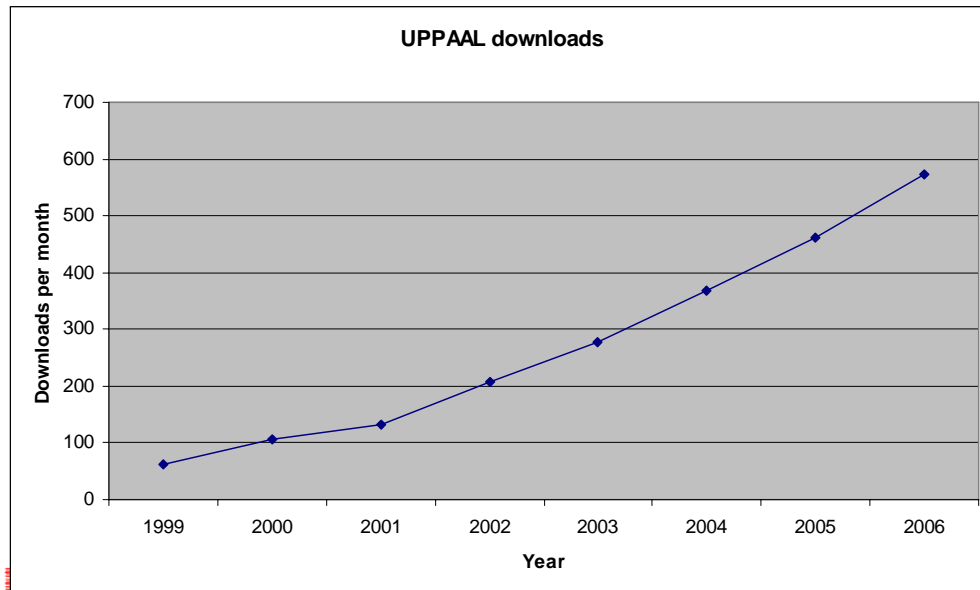
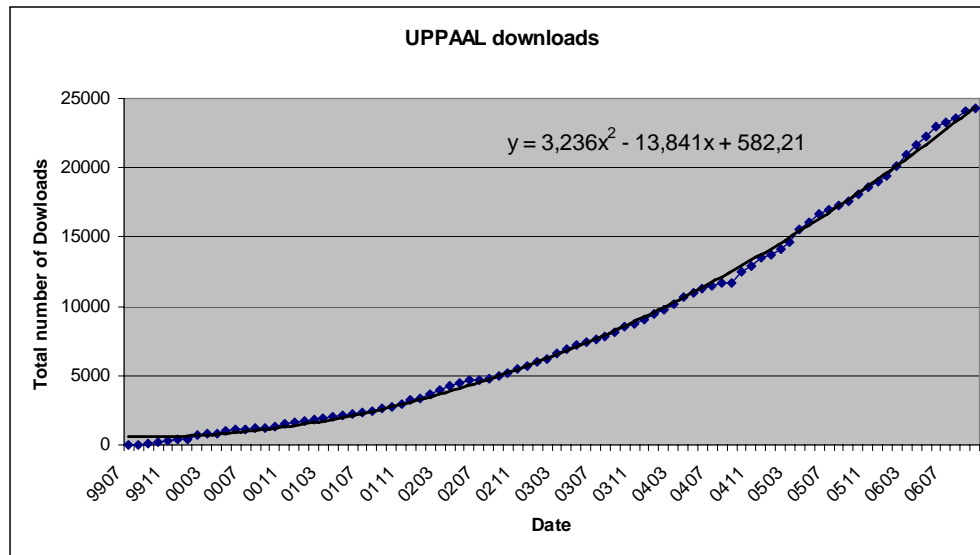
UPPAAL



Verifier

- Exhaustive & automatic checking of requirements
- .. including validating, safety, liveness, bounded liveness and response properties
- .. generation of debugging information for visualisation in simulator.
- Optimal scheduling for cost models

"Impact



Google:

UPPAAL:	134.000
SPIN Verifier:	242.000
nuSMV:	57.700

> 1.500
Google Scholar Citations
(Rhapsody/Esterel < 3.500)

Impact

Academic Courses @

DTU, MCI, IT-U (DK)

Chalmers,

Linköping, Lund,

Chalmers,

Mälardalarn (S)

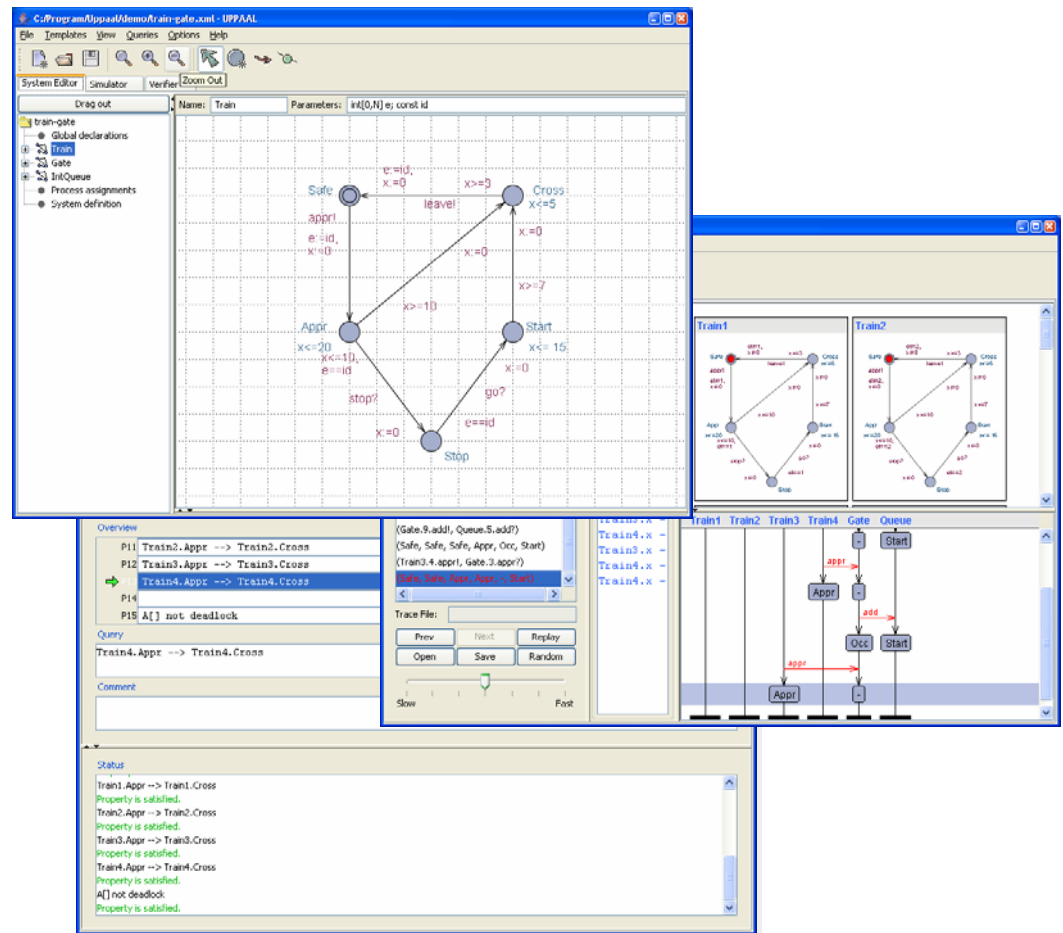
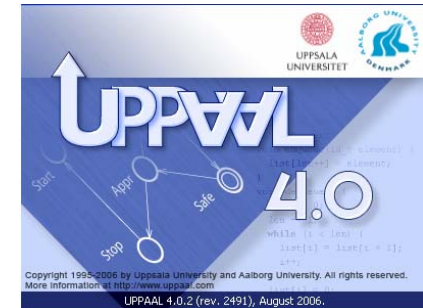
Nijmegen, Twente, CWI
(NL)

Upenn, Northumbria(US)

Braunschweig,

Oldenburg, Marktoberdorf
(D)

Tsinghua, Shanghai, ISS,
NUS (Asia)



Impact

Tutorials Given @

- Estonian School (01)
- IPA Fall D (01)
- FTRTFT (01)
- CPN (02)
- SFM (02)
- MOVEP (01)
- DISC Sch (01)
- MOVEP (01)
- PRISE (01)
- PDMC (01)
- ARTIST2 (01)
- EMSOFT (01)
- RTSS (05)
- TECS week (06)
- TAROT (06)
- ARTS (06)
- GLOBAN (06)
- ARTIST ASIAN SCH (07)

UPPAAL2k: Small Tutorial
日本語版
Ver.1.0

1	イントロダクション	2
2	UPPAAL	2
3	UPPAAL を学ぶ	2
3.1	概要	3
3.2	排他制御アルゴリズム	4
3.3	UPPAAL での時間	7
3.4	Urgent/Committed ロケーション	9
3.5	特性の検証	
3.6	モデリングのトリック	

3.1 概要

UPPAALのメインウィンドウ(図 1) はメニューとタブから構成されています。

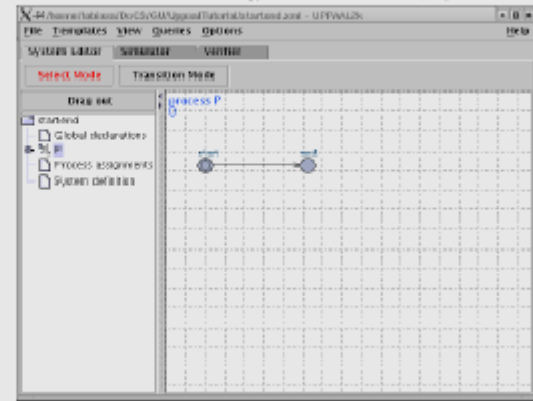
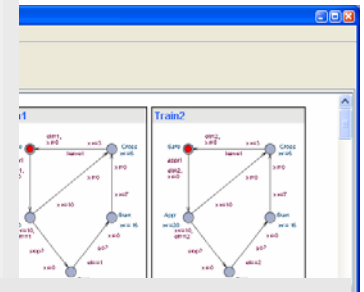
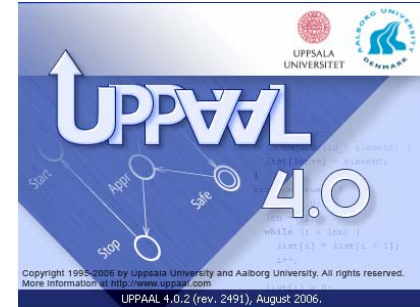


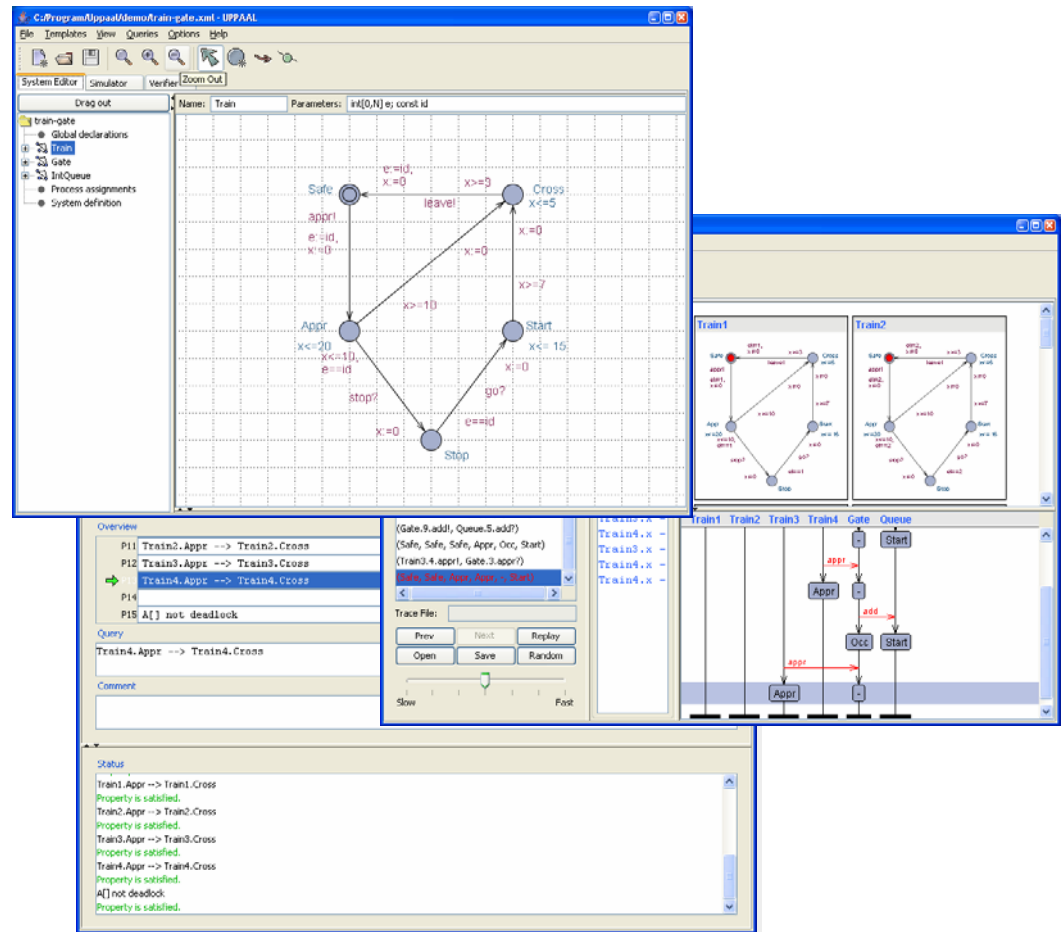
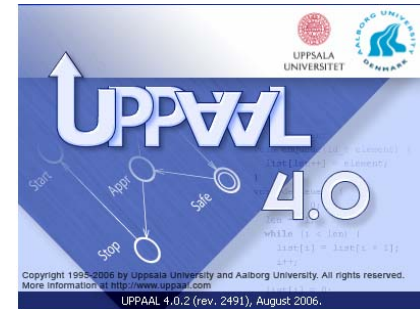
図 1: UPPAAL の画面



Impact

Company Downloads

- Mecel
- Jet
- Symantec
- SRI
- Relogic
- Realwork
- NASA
- Verified Systems
- Microsoft
- ABB
- Airbus
- PSA
- Saab
- Siemens
- Volvo
- Lucent Technologies



Timed Automata

Alur & Dill 1989



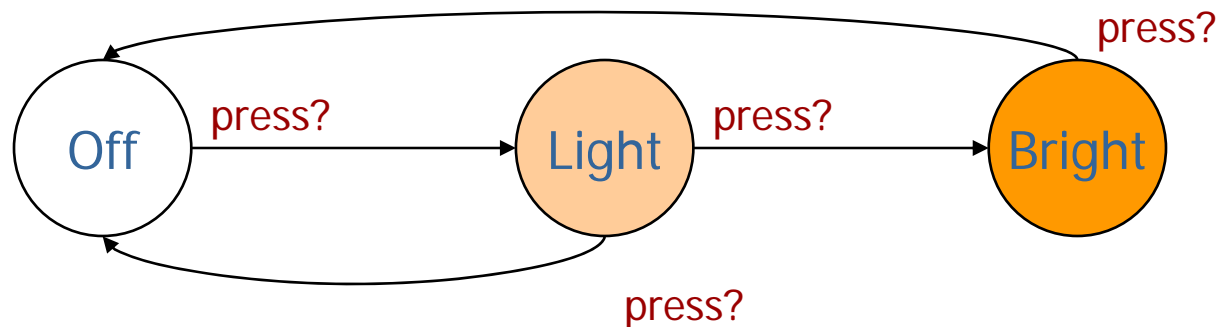
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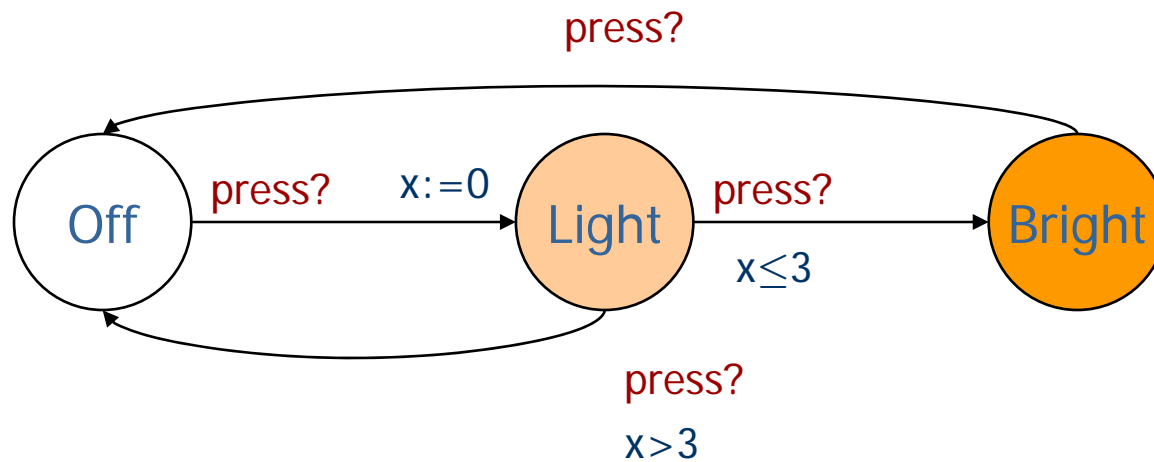
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Dumb Light Control



WANT: if **press** is issued twice **quickly** then the **light** will get **brighter**; otherwise the light is turned **off**.

Dumb Light Control *Alur & Dill 1990*



Solution: Add real-valued clock **x**

Timed Automata *review*

Alur & Dill 1990

Clocks:

Guard

Boolean combination of **integer bounds** on **clocks**

Reset

Action performed on clocks

State

(*location* , $x=v$, $y=u$) where v,u are in \mathbf{R}

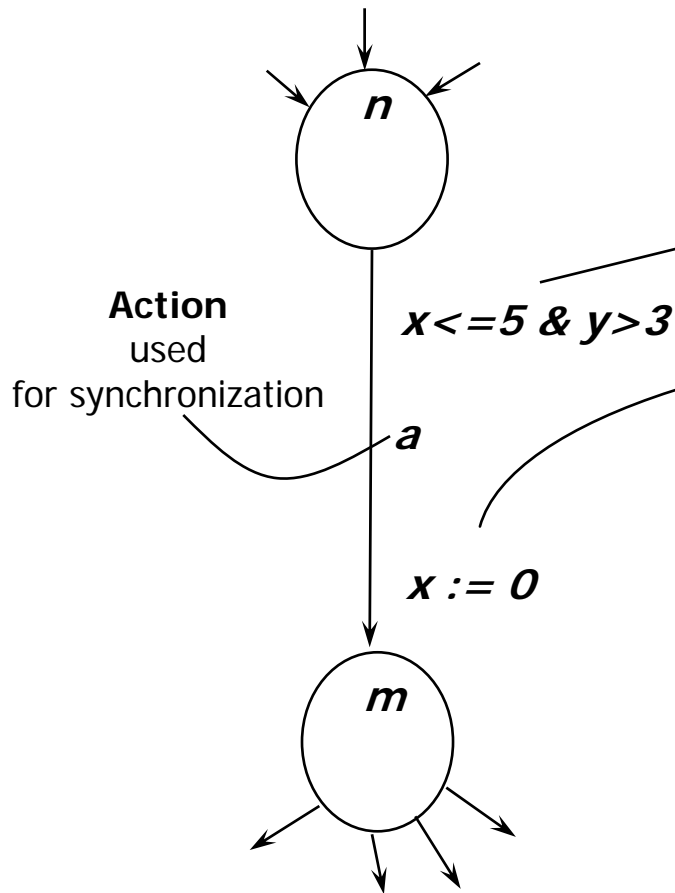
Transitions

Discrete Trans

$(n , x=2.4 , y=3.1415) \xrightarrow{a} (m , x=0 , y=3.1415)$

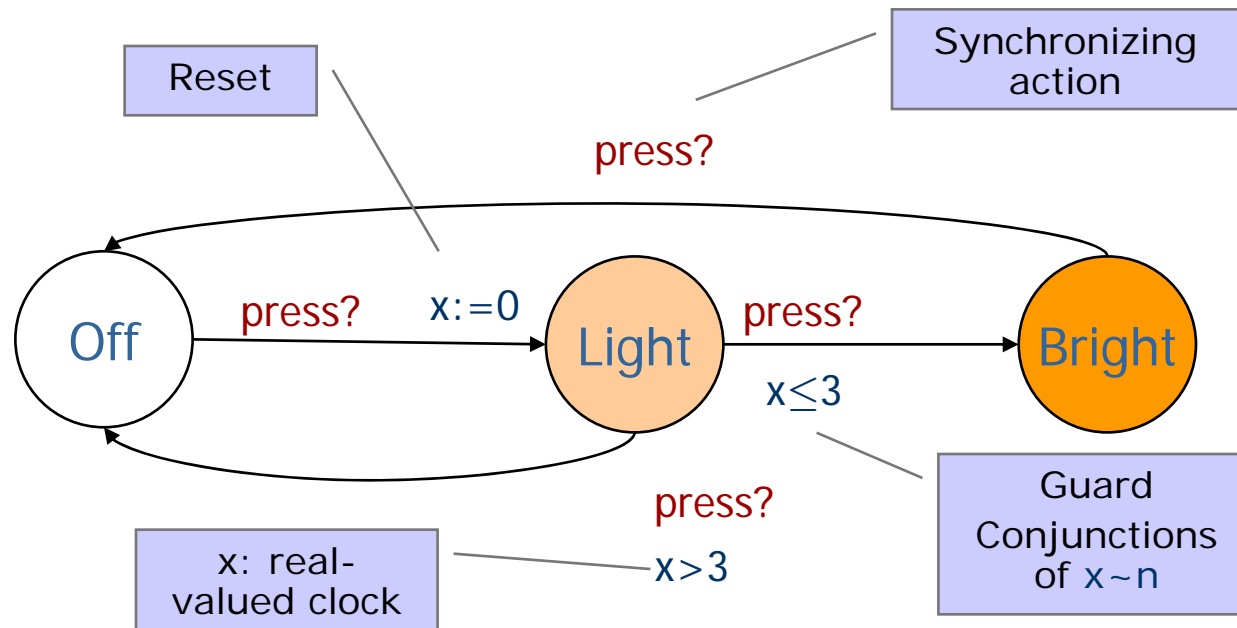
Delay Trans

$(n , x=2.4 , y=3.1415) \xrightarrow{e(1.1)} (n , x=3.5 , y=4.2415)$



Timed Automata

Alur & Dill 1990

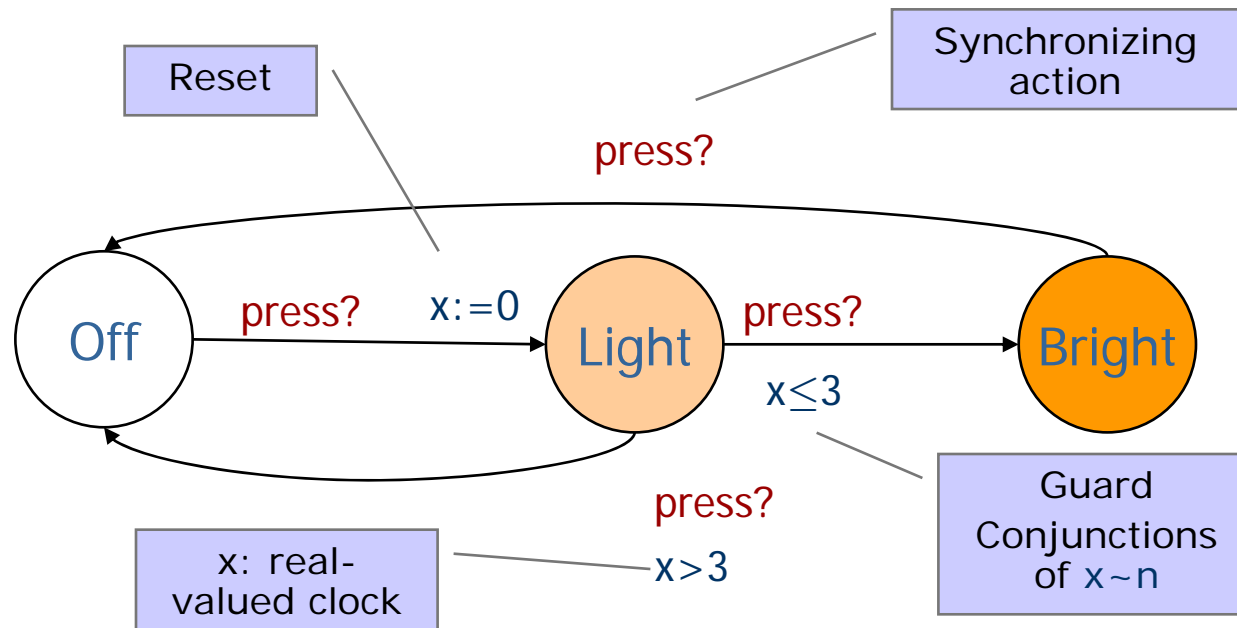


States:
 (location , $x=v$) where $v \in \mathbf{R}$

Transitions:
 (Off , $x=0$)

Timed Automata

Alur & Dill 1990

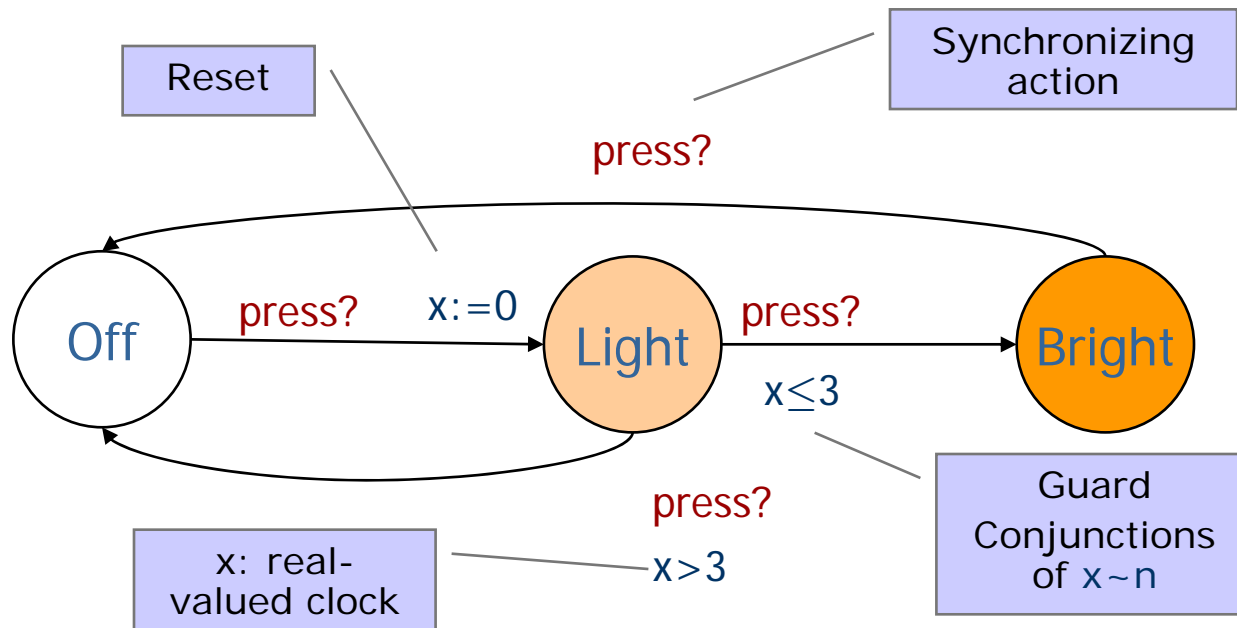


States:
(location , $x=v$) where $v \in \mathbf{R}$

Transitions:
 delay 4.32 (Off , $x=0$)
 → (Off , $x=4.32$)

Timed Automata

Alur & Dill 1990



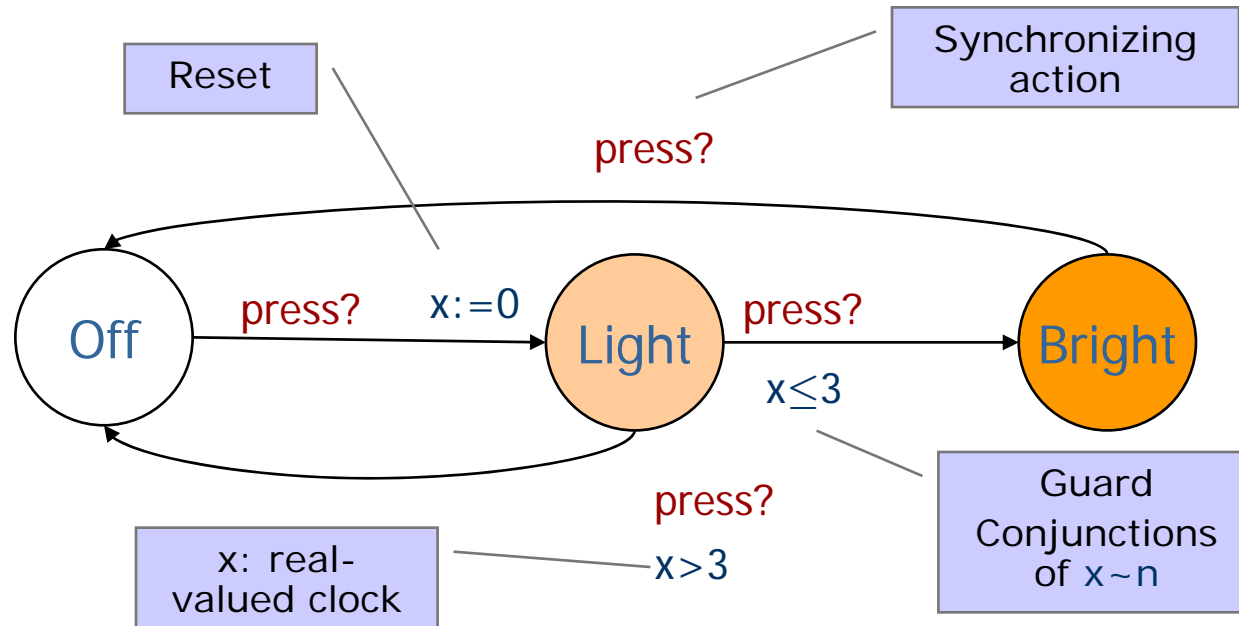
States:
 (location , $x=v$) where $v \in \mathbf{R}$

Transitions:

	(Off , $x=0$)
delay 4.32	\rightarrow (Off , $x=4.32$)
press?	\rightarrow (Light , $x=0$)

Timed Automata

Alur & Dill 1990



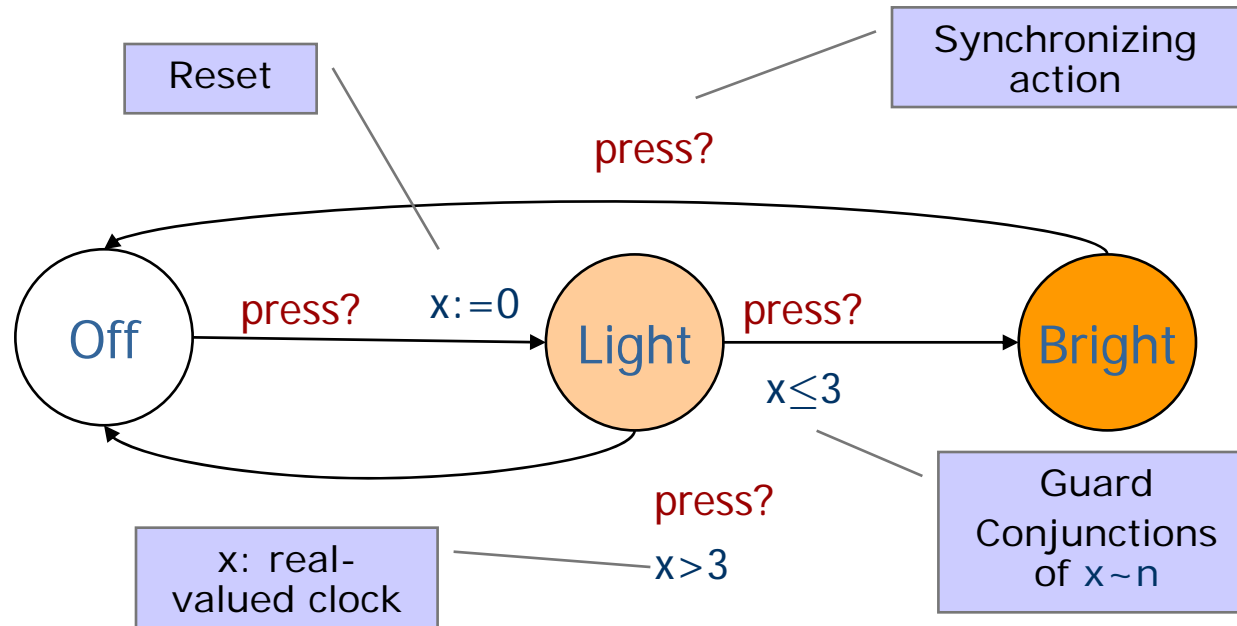
States:
 (location , $x=v$) where $v \in \mathbf{R}$

Transitions:

	(Off , $x=0$)
delay 4.32	\rightarrow (Off , $x=4.32$)
$press?$	\rightarrow (Light , $x=0$)
delay 2.51	\rightarrow (Light , $x=2.51$)

Timed Automata

Alur & Dill 1990



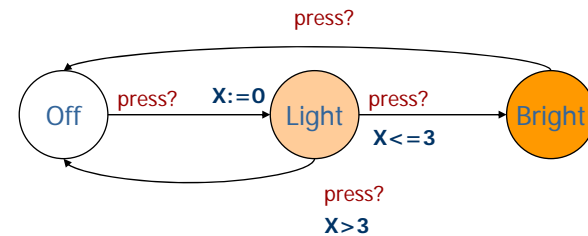
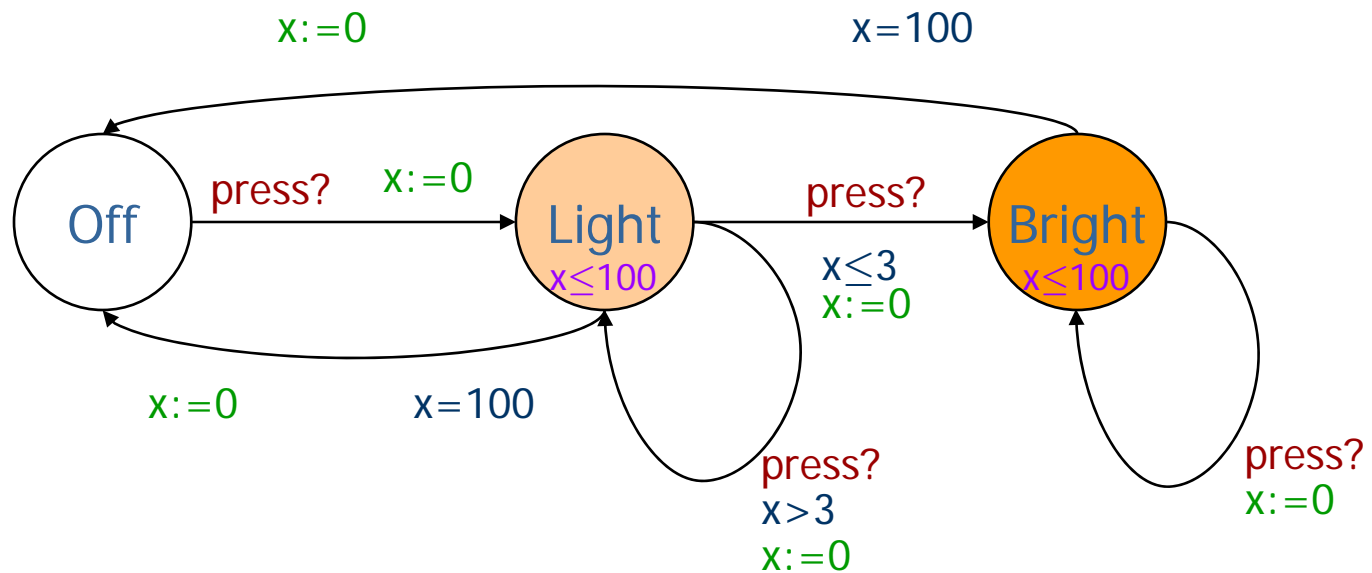
States:
(location , $x=v$) where $v \in \mathbf{R}$

Transitions:

	(Off , $x=0$)
delay 4.32	\rightarrow (Off , $x=4.32$)
press?	\rightarrow (Light , $x=0$)
delay 2.51	\rightarrow (Light , $x=2.51$)
press?	\rightarrow (Bright , $x=2.51$)

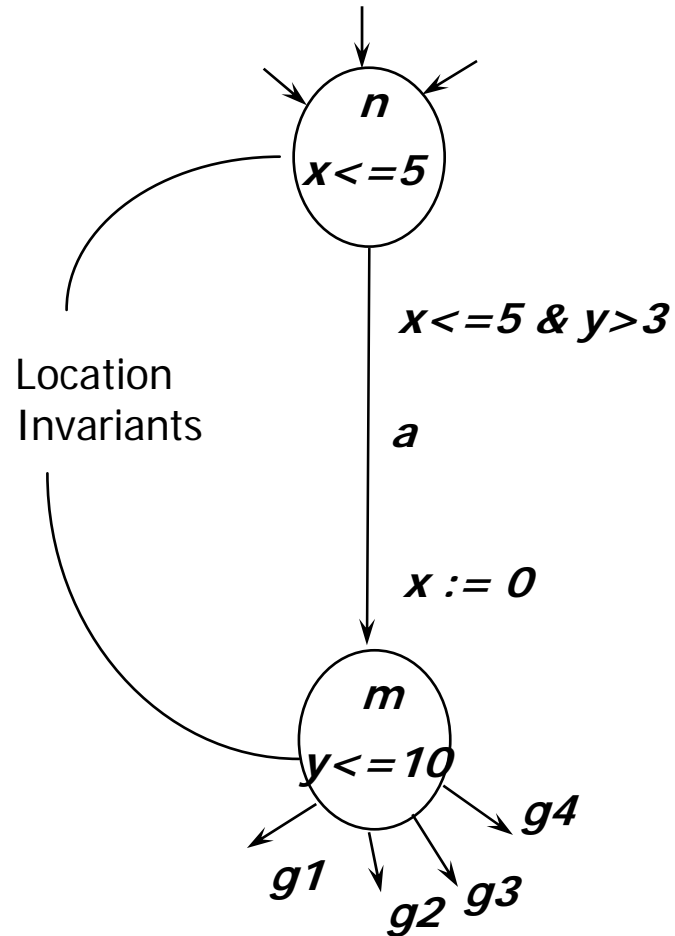
Intelligent Light Control

Using Invariants



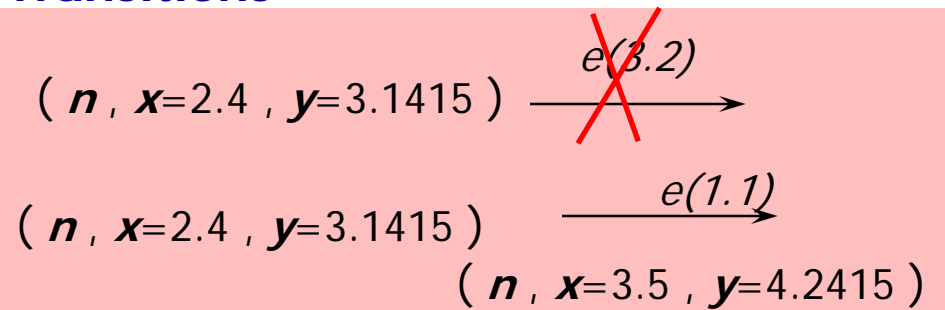
Timed Automata *review*

Invariants



Clocks: x, y

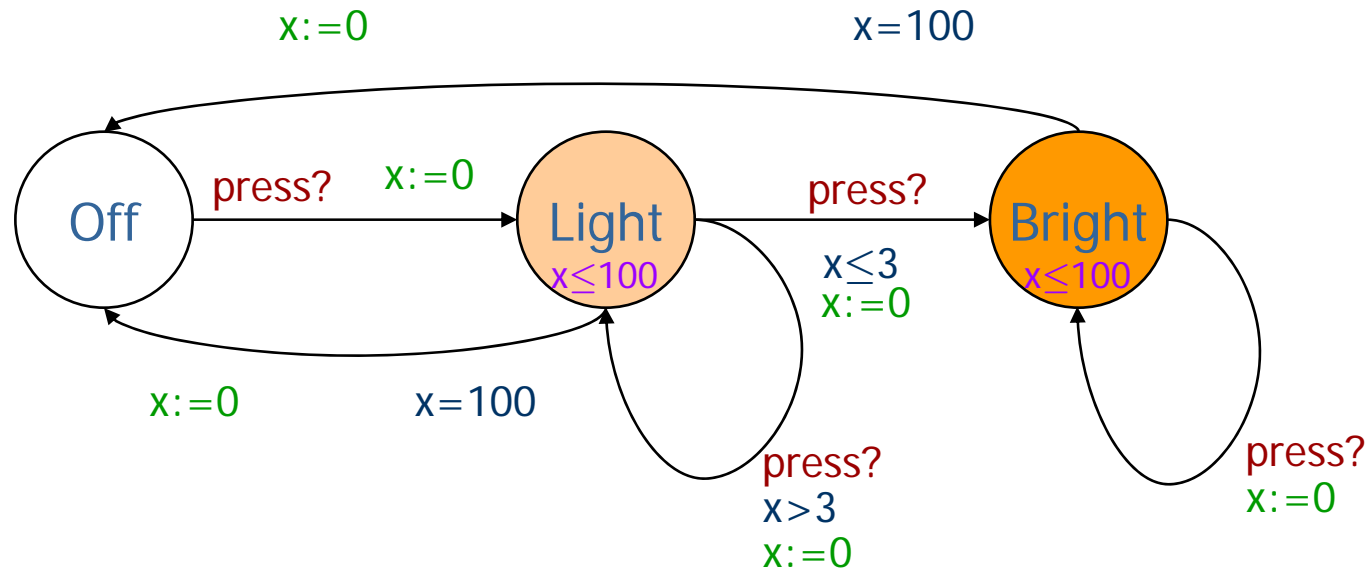
Transitions



**Invariants
ensure
progress!!**

Intelligent Light Control

Using Invariants



Transitions:

	(Off , x=0)
delay 4.32	→ (Off , x=4.32)
press?	→ (Light , x=0)
delay 4.51	→ (Light , x=4.51)
press?	→ (Light , x=0)
delay 100	→ (Light , x=100)
τ	→ (Off , x=0)

Note:

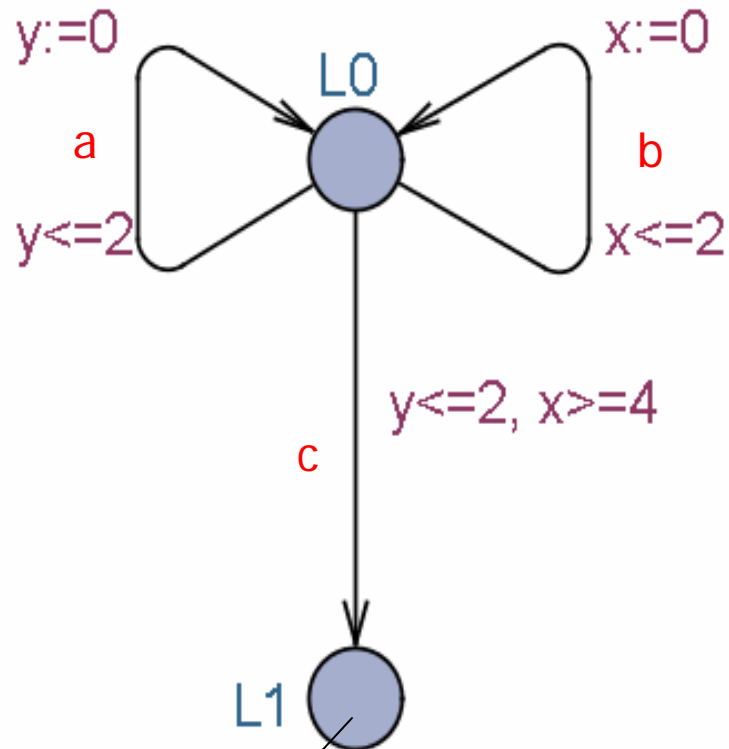
(Light , x=0) delay 103 →



Invariants
ensures
progress

Example

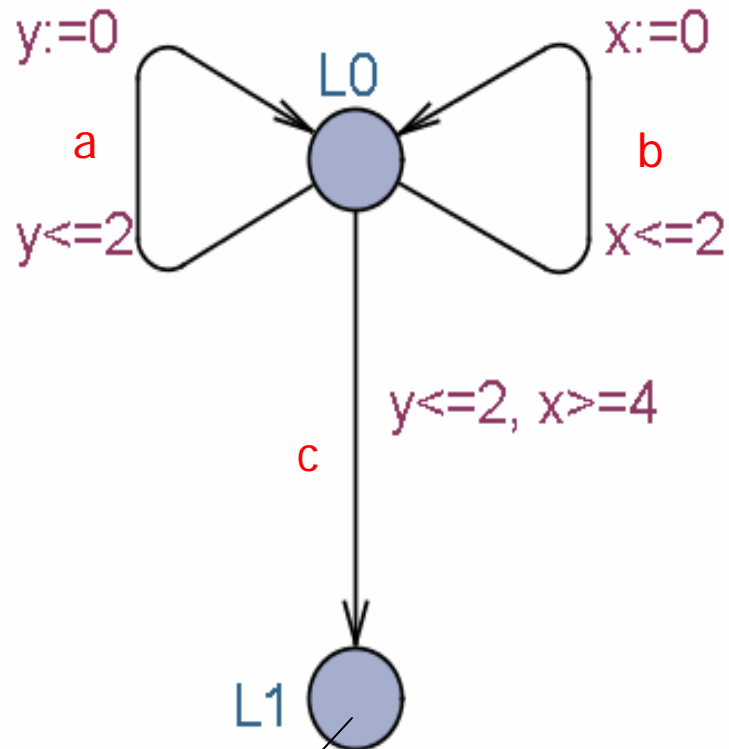
With two clocks



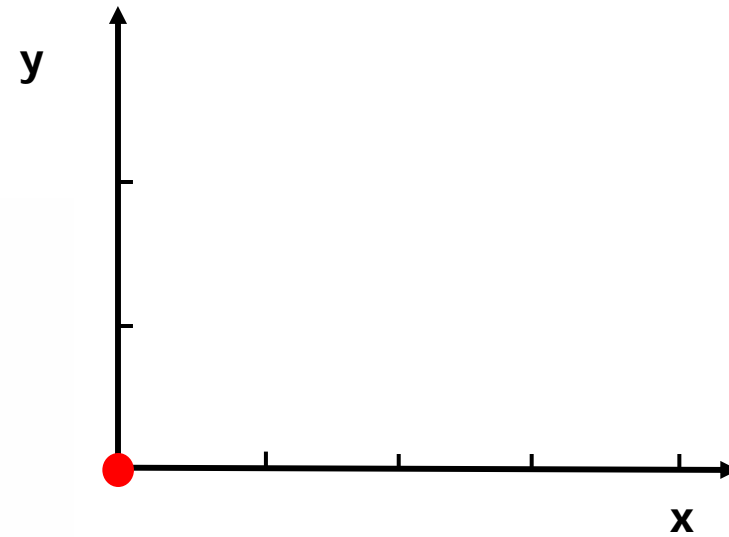
Reachable?

Example

With two clocks



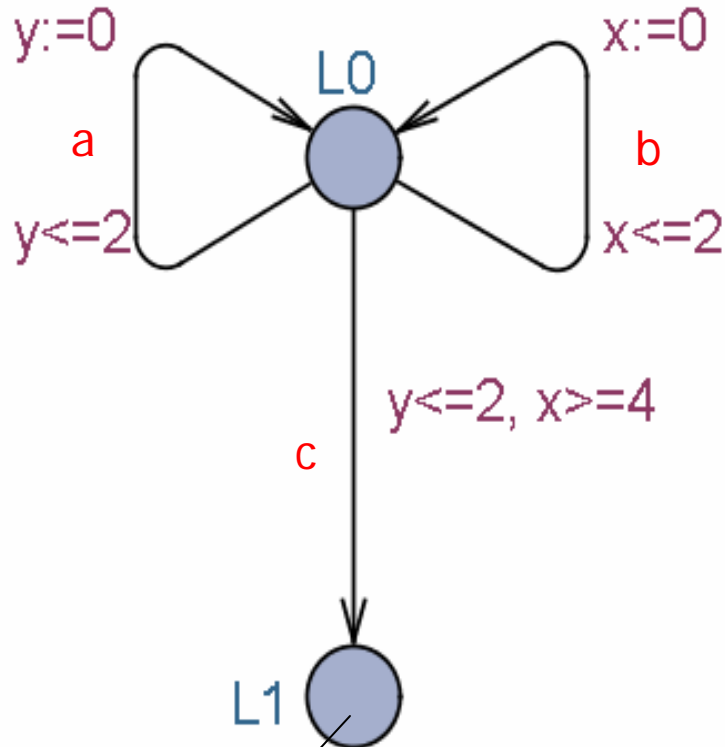
Reachable?



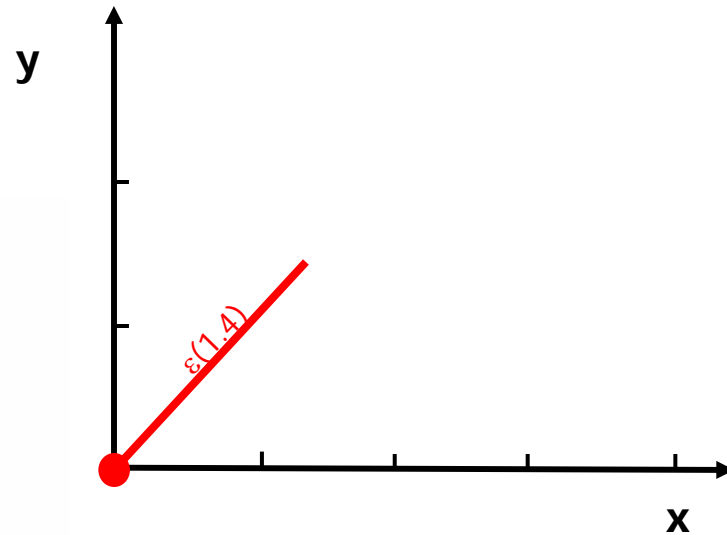
$(L0, x=0, y=0)$

Example

With two clocks



Reachable?



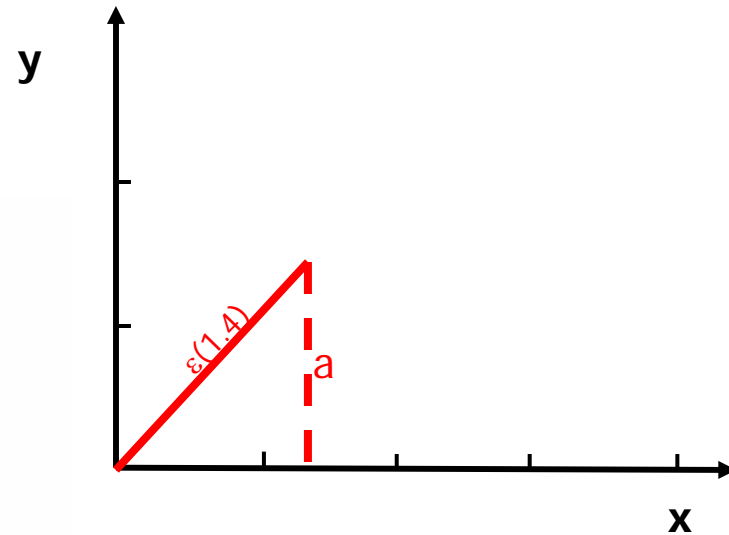
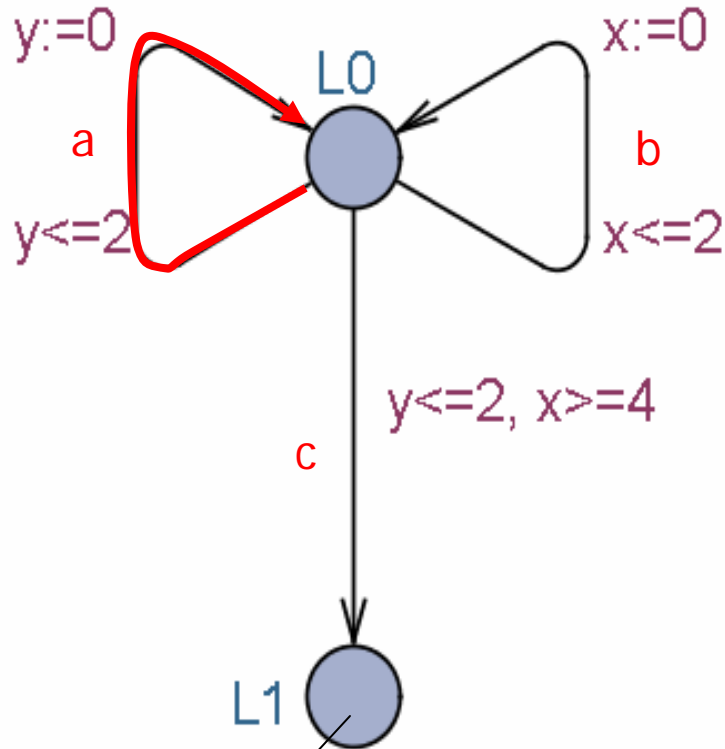
$(L0, x=0, y=0)$

$\rightarrow_{\epsilon(1.4)}$

$(L0, x=1.4, y=1.4)$

Example

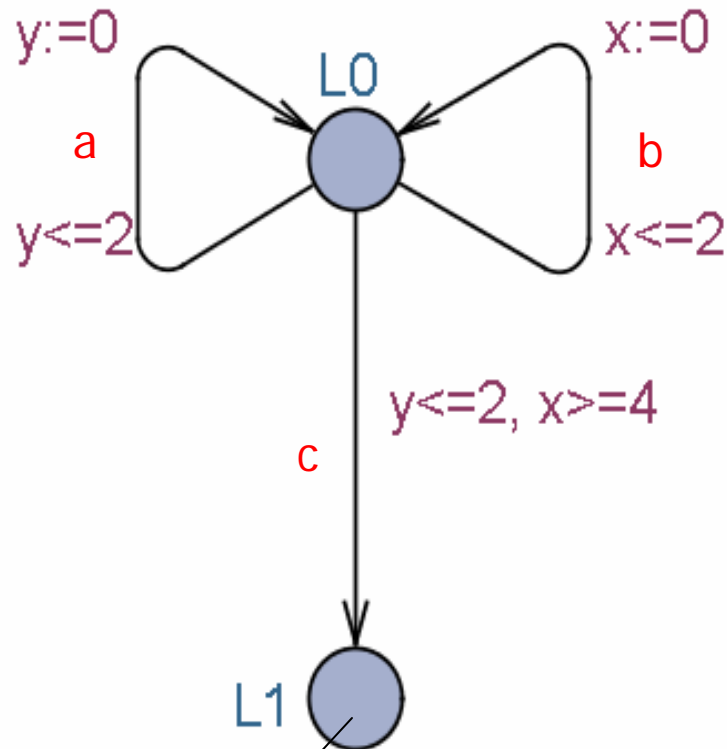
With two clocks



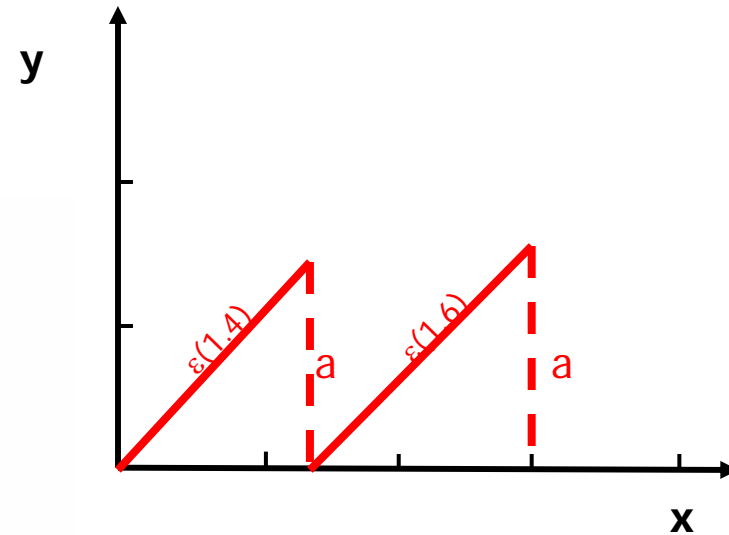
$(L0, x=0, y=0)$
 $\rightarrow_{\epsilon(1.4)}$
 $(L0, x=1.4, y=1.4)$
 \rightarrow_a
 $(L0, x=1.4, y=0)$

Example

With two clocks



Reachable?



$(L0, x=0, y=0)$

$\rightarrow_{\epsilon(1.4)}$

$(L0, x=1.4, y=1.4)$

\rightarrow_a

$(L0, x=1.4, y=0)$

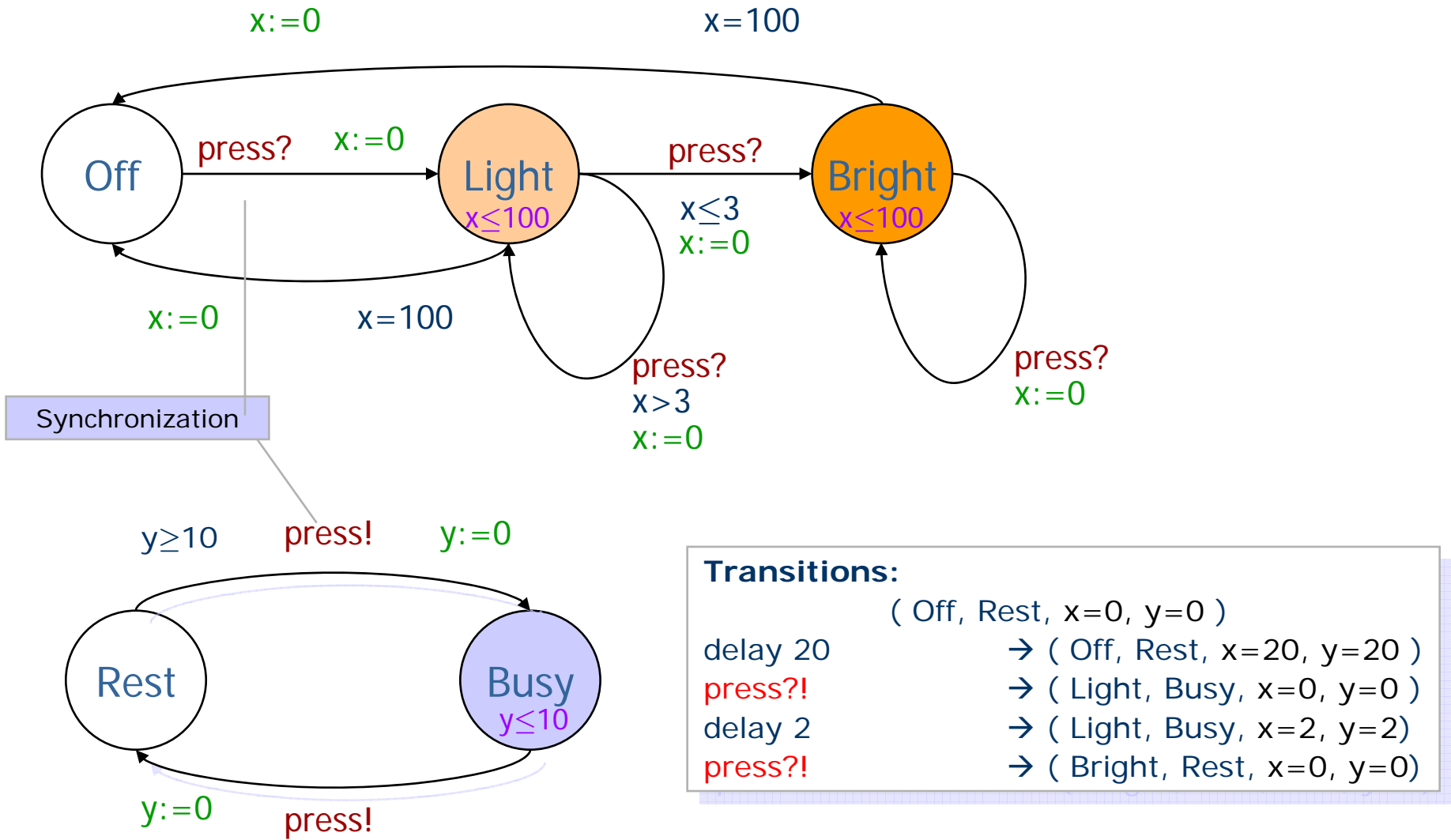
$\rightarrow_{\epsilon(1.6)}$

$(L0, x=3.0, y=1.6)$

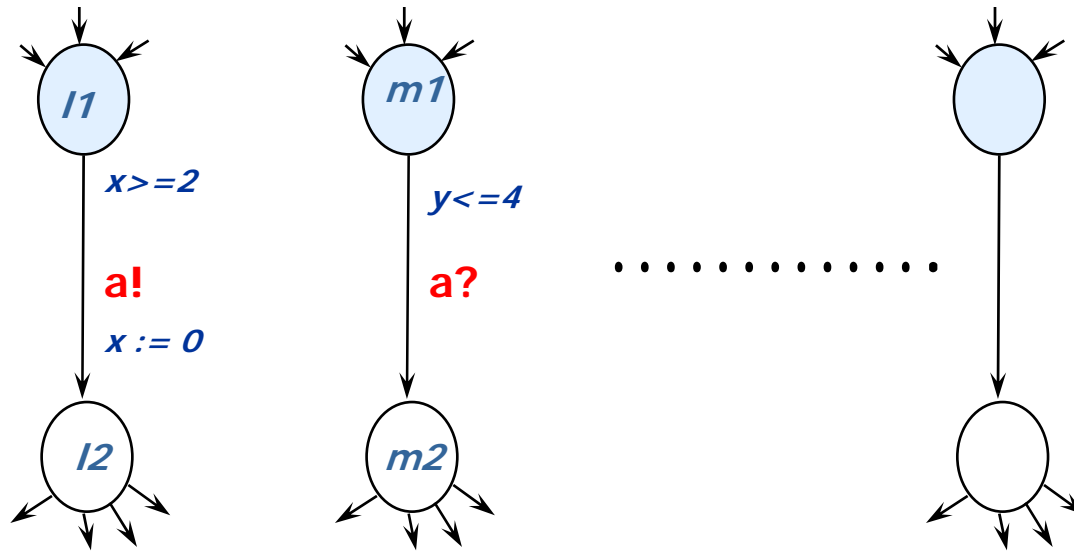
\rightarrow_a

$(L0, x=3.0, y=0)$

Networks Light Controller & User

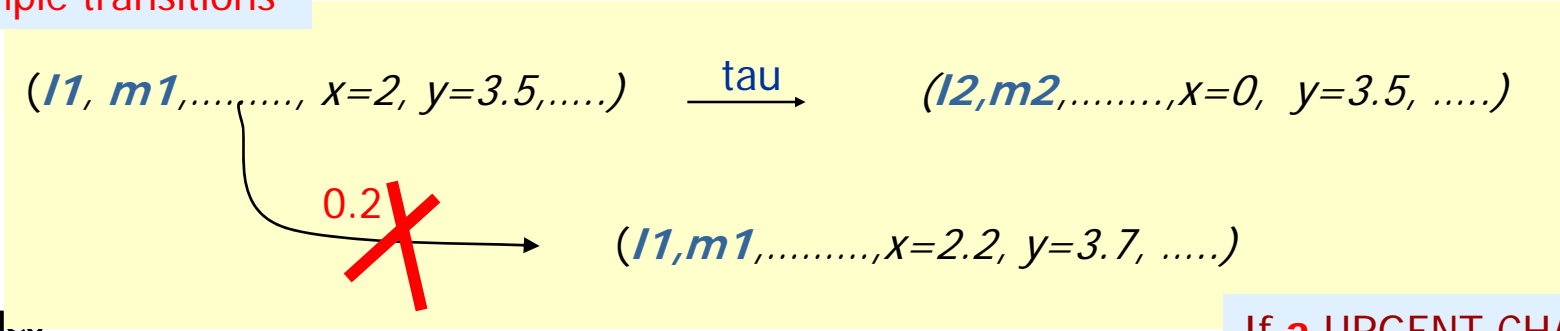


Networks of Timed Automata (a'la CCS)



Two-way synchronization on *complementary* actions.
Closed Systems!

Example transitions



If **a** URGENT CHANNEL

Timed Automata

Formally



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Constraints

Definition

Let X be a set of clock variables. The set $\mathcal{B}(X)$ of *clock constraints* ϕ is given by the grammar:

$$\phi ::= x \leq c \mid c \leq x \mid x < c \mid c < x \mid \phi_1 \wedge \phi_2$$

where $c \in \mathbb{N}$ (or \mathbb{Q}).

Clock Valuations and Notation

Definition

The set of *clock valuations*, \mathbb{R}^C is the set of functions $C \rightarrow \mathbb{R}_{\geq 0}$ ranged over by u, v, w, \dots

Notation

Let $u \in \mathbb{R}^C$, $r \subseteq C$, $d \in \mathbb{R}_{\geq 0}$, and $g \in \mathcal{B}(X)$ then:

- $u + d \in \mathbb{R}^C$ is defined by $(u + d)(x) = u(x) + d$ for any clock x
- $u[r] \in \mathbb{R}^C$ is defined by $u[r](x) = 0$ when $x \in r$ and $u[r](x) = u(x)$ for $x \notin r$.
- $u \models g$ denotes that g is satisfied by u .

Timed Automata

Definition

A timed automaton A over clocks C and actions Act is a tuple (L, l_0, E, I) , where:

- L is a finite set of locations
- $l_0 \in L$ is the initial location
- $E \subseteq L \times \mathcal{B}(X) \times Act \times \mathcal{P}(C) \times L$ is the set of edges
- $I : L \rightarrow \mathcal{B}(X)$ assigns to each location an invariant

Semantics

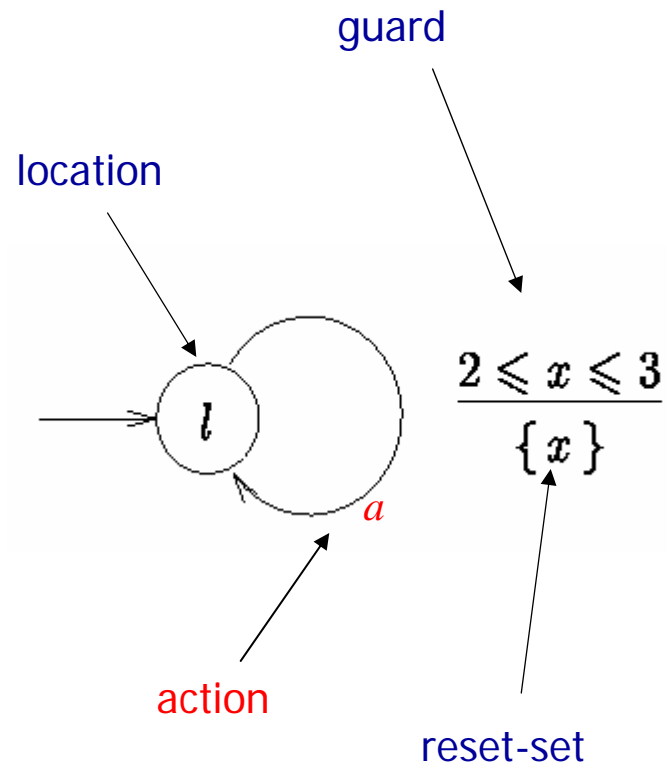
Definition

The semantics of a timed automaton A is a labelled transition system with state space $L \times \mathbb{R}^C$ with initial state $(l_0, u_0)^*$ and with the following transitions:

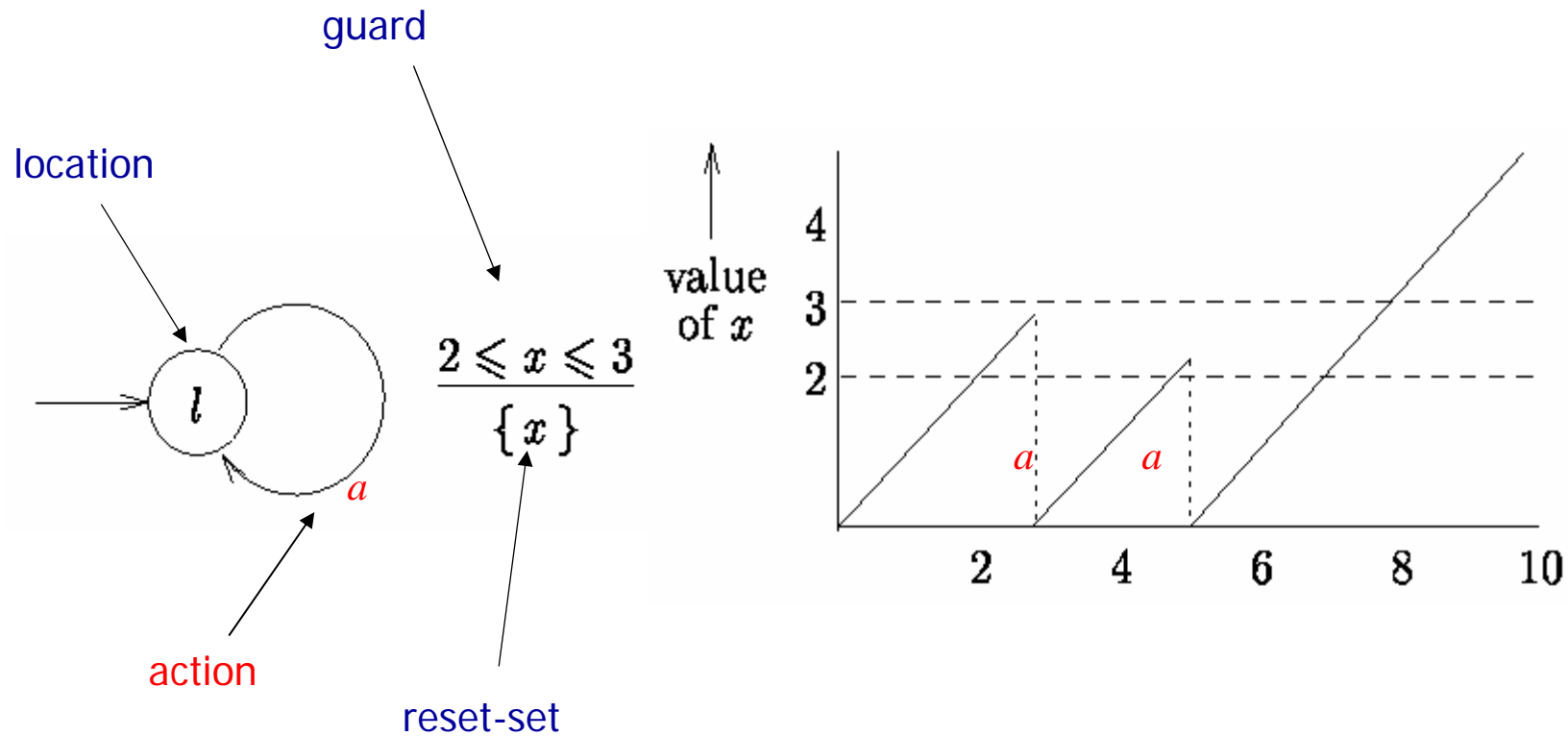
- $(l, u) \xrightarrow{\epsilon(d)} (l, u + d)$ iff $u \in I(l)$ and $u + d \in I(l)$,
- $(l, u) \xrightarrow{a} (l', u')$ iff there exists $(l, g, a, r, l') \in E$ such that
 - $u \models g$,
 - $u' = u[r]$, and
 - $u' \in I(l')$

* $u_0(x) = 0$ for all $x \in C$

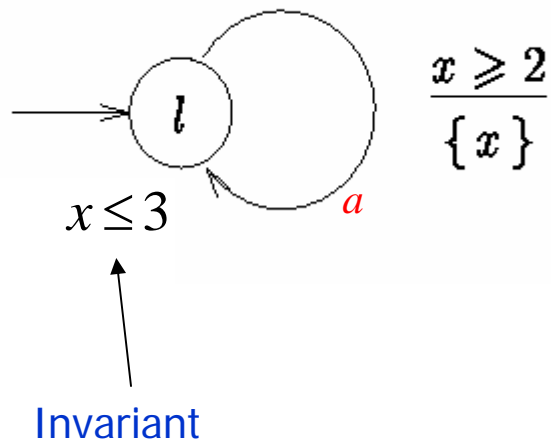
Timed Automata: Example



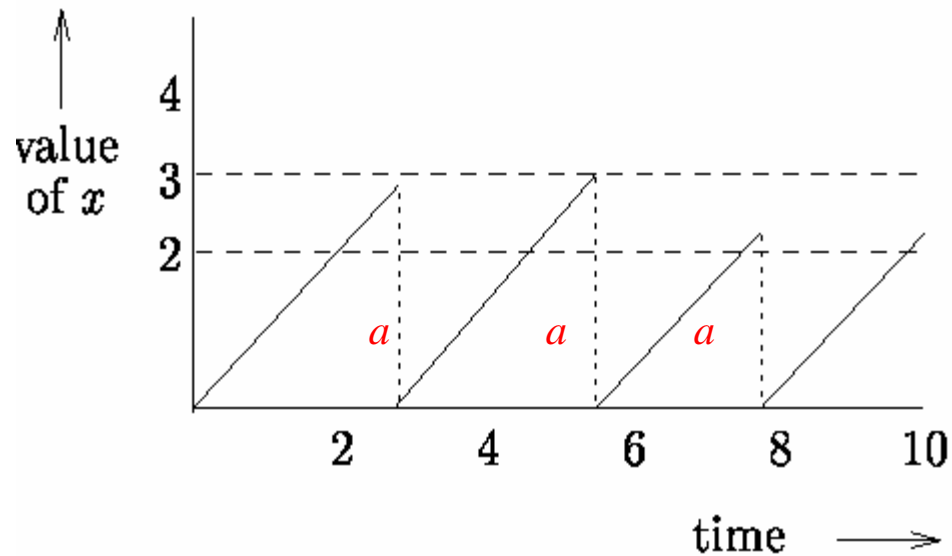
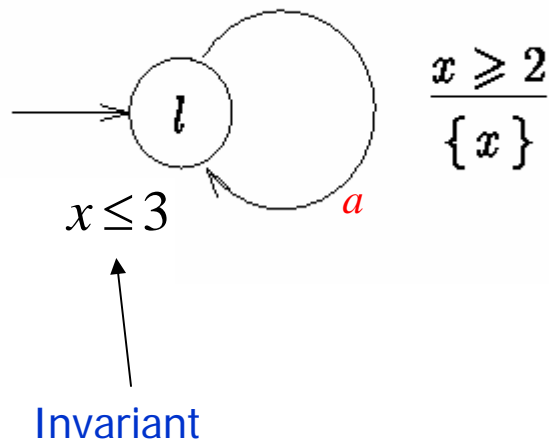
Timed Automata: Example



Timed Automata: Example



Timed Automata: Example



Brick Sorting



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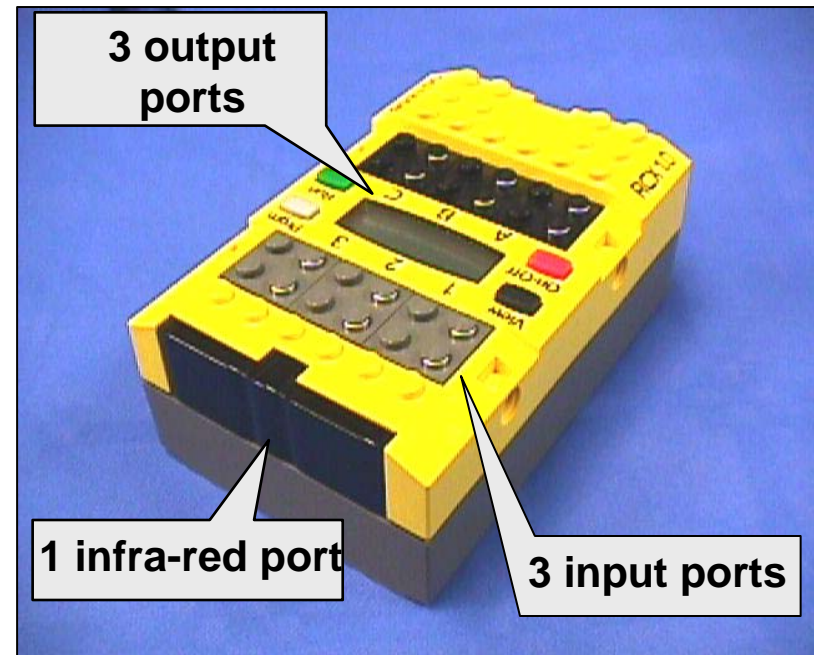
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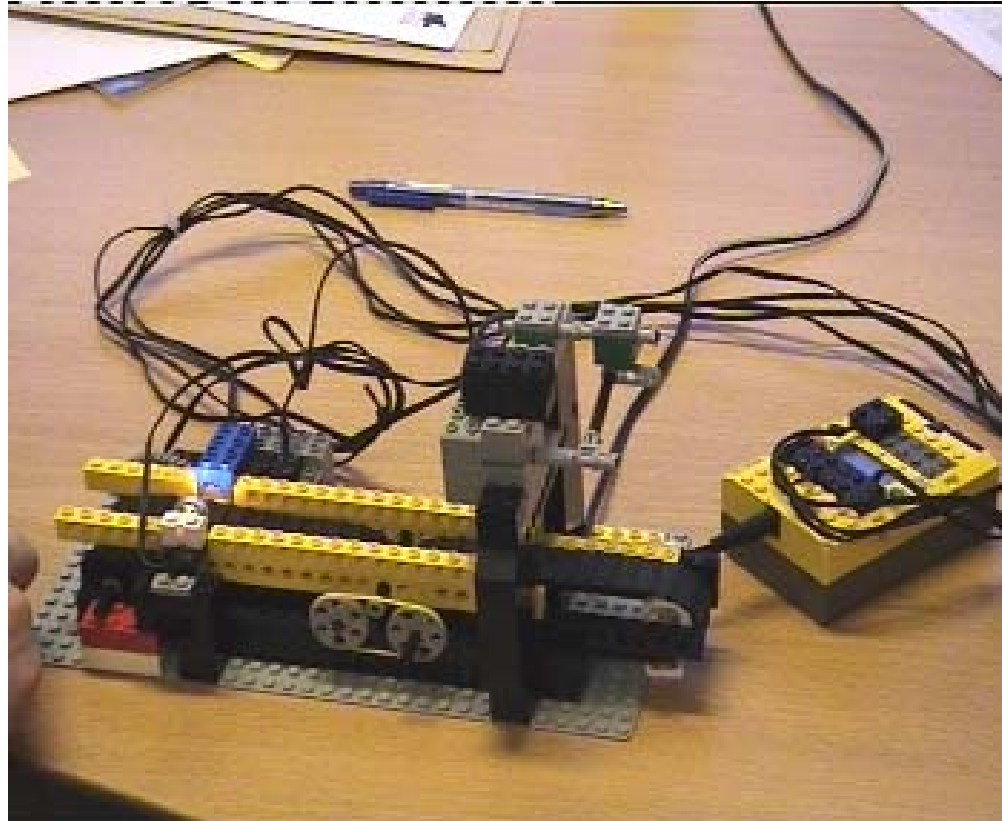
LEGO Mindstorms/RCX

- Sensors: temperature, light, rotation, pressure.
- Actuators: motors, lamps,
- Virtual machine:
 - 10 tasks, 4 timers, 16 integers.
- Several Programming Languages:
 - NotQuiteC, Mindstorm, Robotics, legOS, etc.



A Real Real Timed System

The Plant
Conveyor Belt
&
Bricks

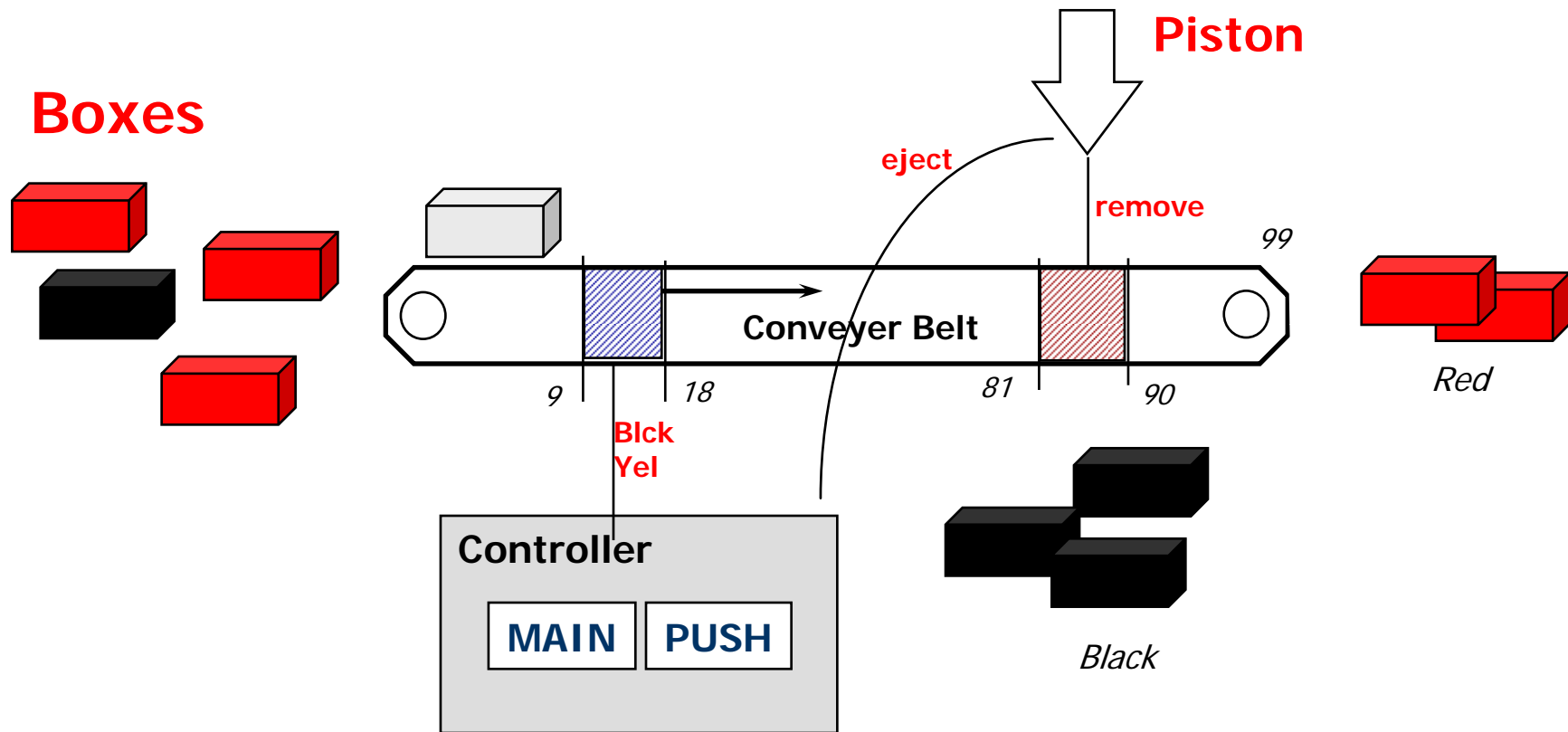


**Controller
Program**
LEGO MINDSTORM

First UPPAAL model

Sorting of Lego Boxes

Ken Tindell



Exercise: Design **Controller** so that **black** boxes are being pushed out

NQC programs

```
int active;
int DELAY;
int LIGHT_LEVEL;
```

```
task MAIN{
  DELAY=75;
  LIGHT_LEVEL=35;
  active=0;
  Sensor(IN_1, IN_LIGHT);
  Fwd(OUT_A,1);
  Display(1);

  start PUSH;

  while(true){

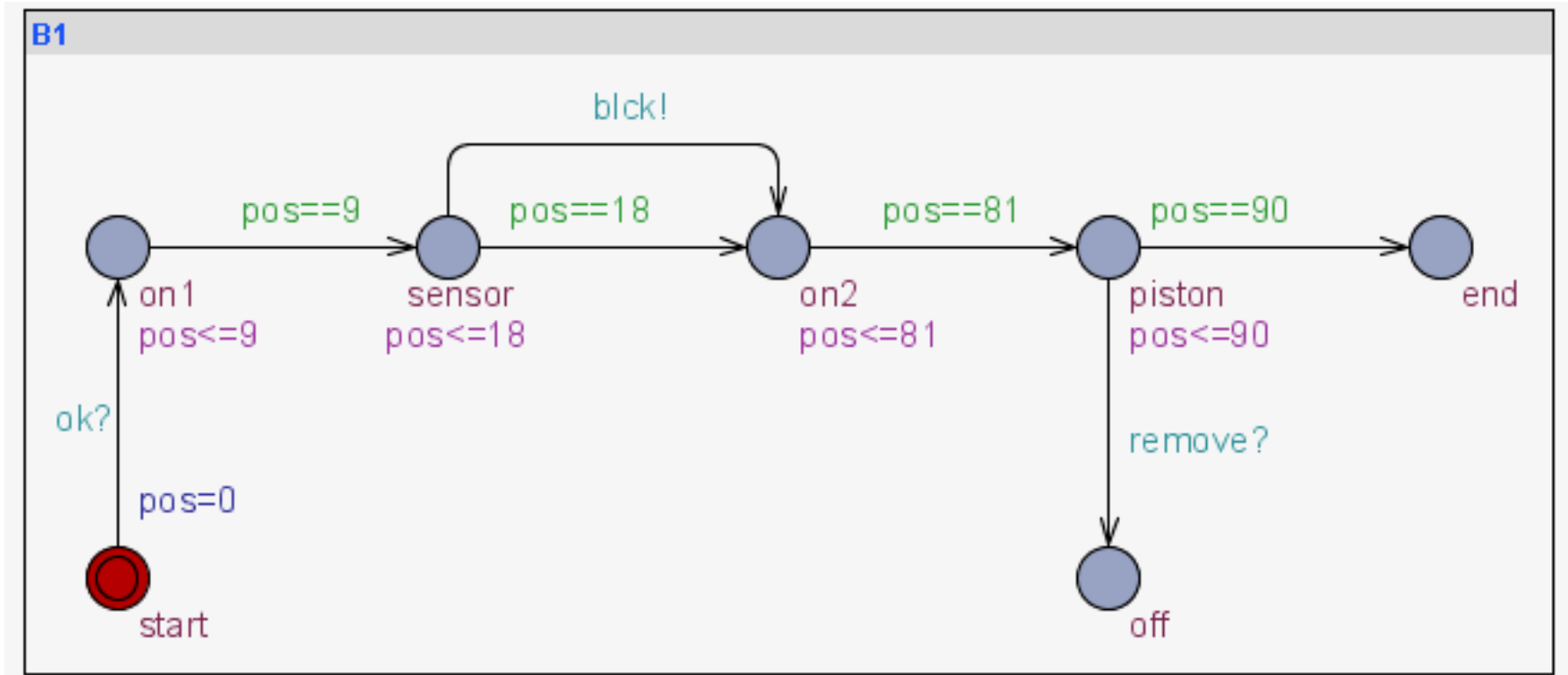
wait(IN_1<=LIGHT_LEVEL);
  ClearTimer(1);
  active=1;
  PlaySound(1);

wait(IN_1>LIGHT_LEVEL);
  }
}
```

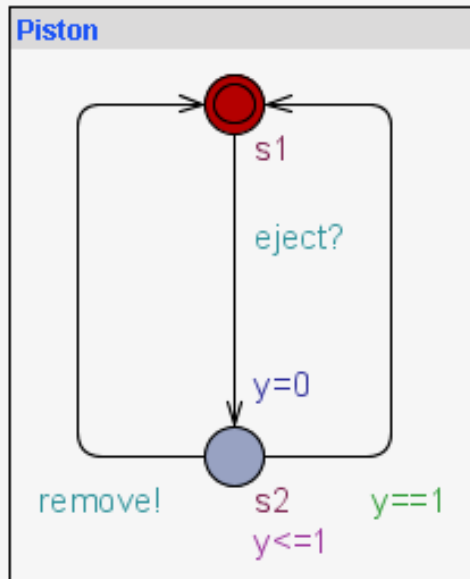
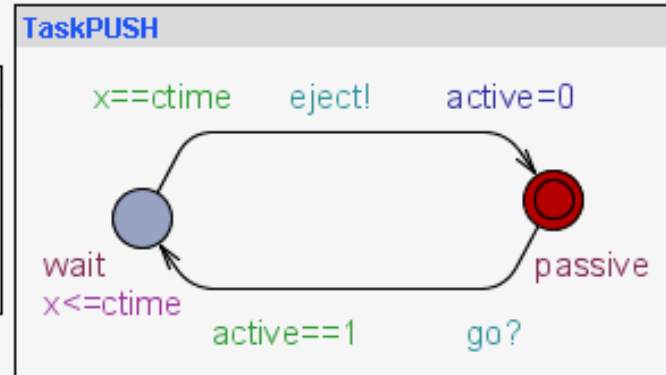
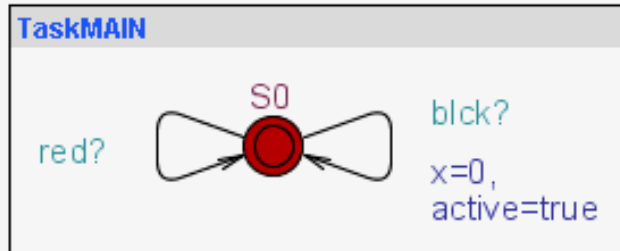
```
task PUSH{
  while(true){
    wait(Timer(1)>DELAY && active==1);
    active=0;
    Rev(OUT_C,1);
    Sleep(8);
    Fwd(OUT_C,1);
    Sleep(12);
    Off(OUT_C);
  }
}
```



A Black Brick



Control Tasks & Piston



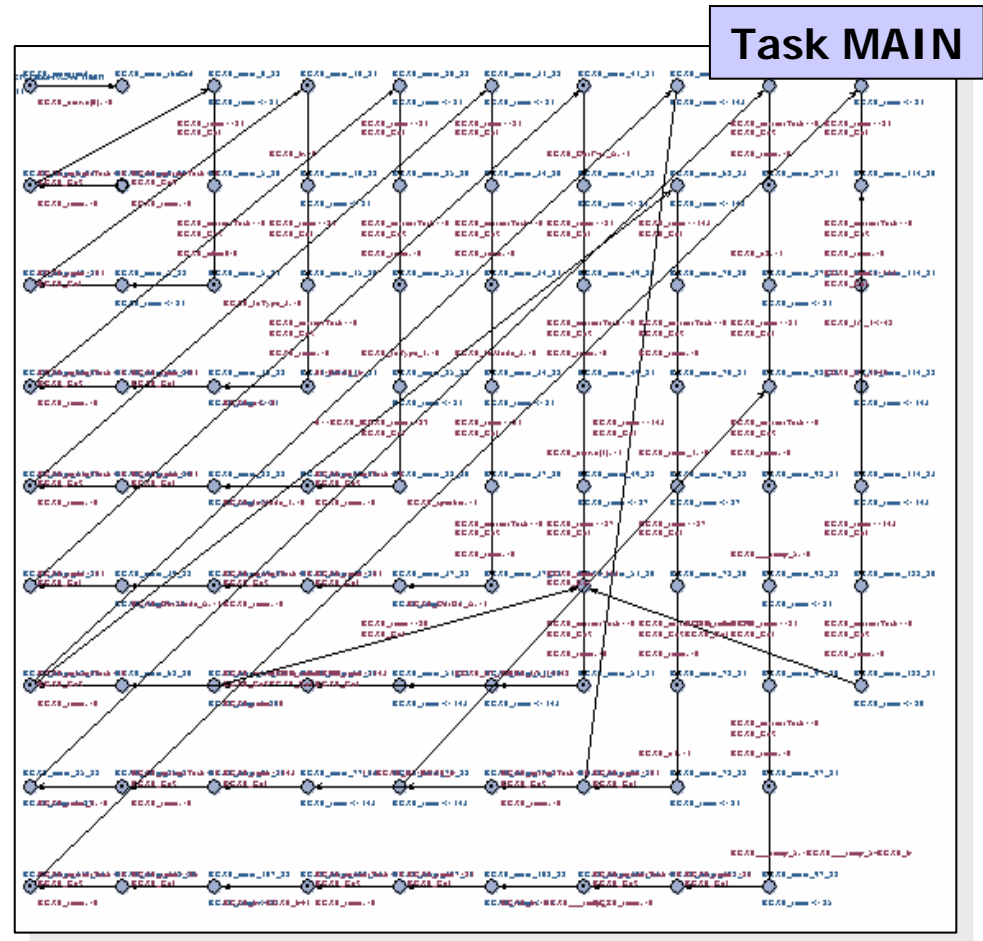
GLOBAL DECLARATIONS:
 const **int** ctime = 75;

int[0,1] active;
clock x, time;

chan eject, ok;
urgent chan blk, red, remove, go;

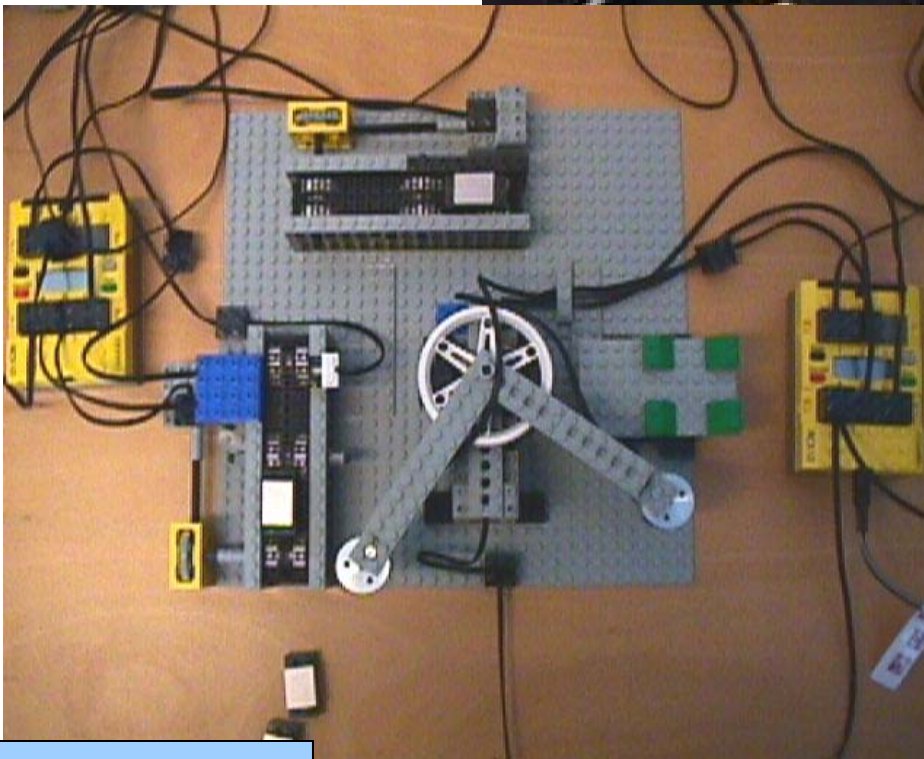
From RCX to UPPAAL – and back

- Model includes Round-Robin Scheduler.
- Compilation of RCX tasks into TA models.
- Presented at ECRTS 2000 in Stockholm.
- From UPPAAL to RCX: Martijn Hendriks.

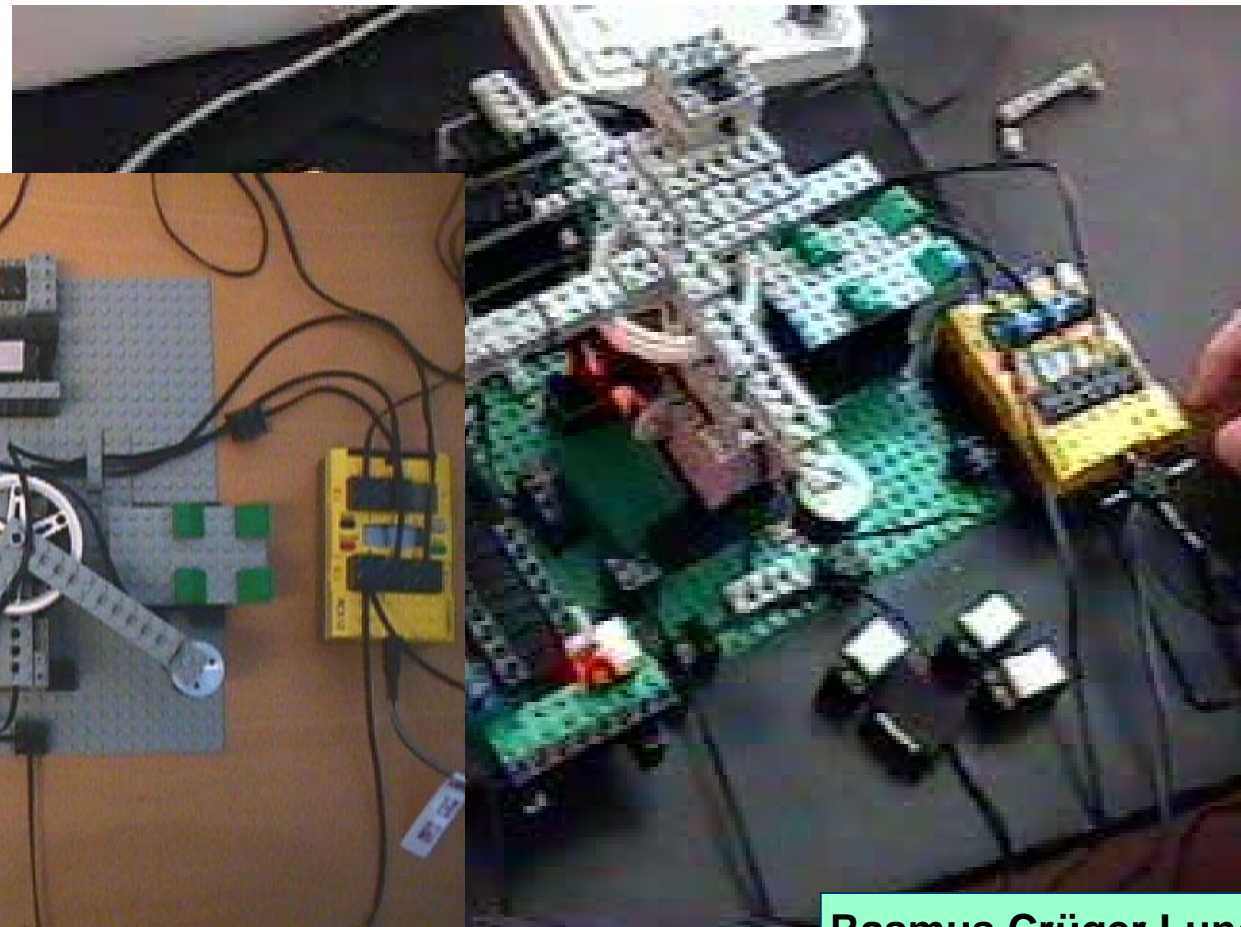


The Production Cell in LEGO

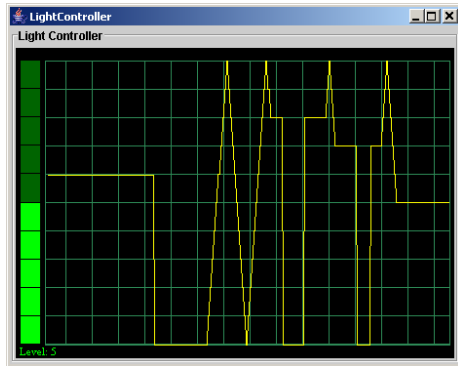
Course at DTU, Copenhagen



Production Cell



Rasmus Crüger Lund
Simon Tune Riemanni



Light Control Interface



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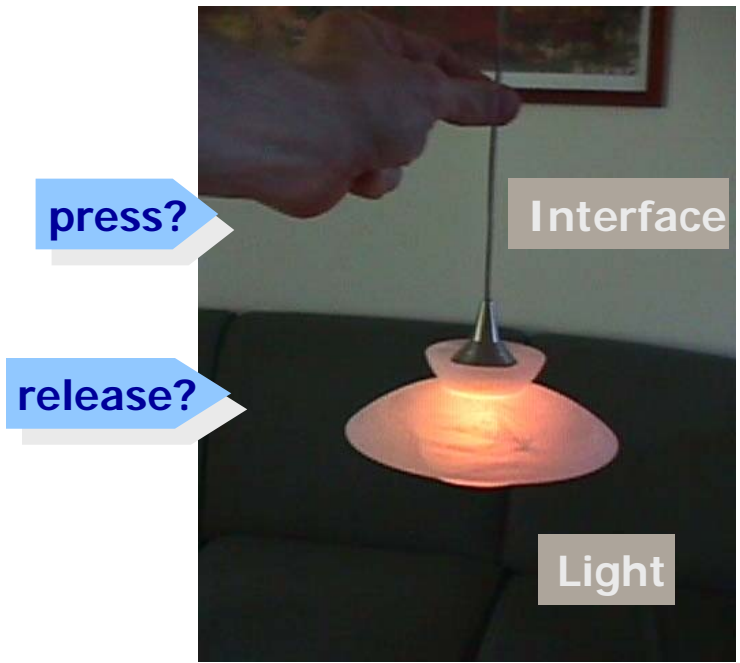


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Light Control Interface



User



press?

release?

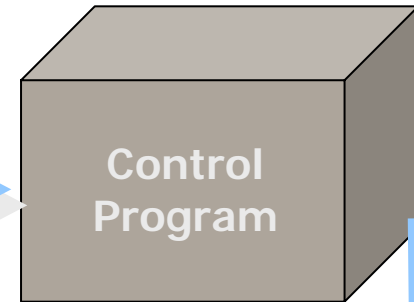
Interface

Light

touch!

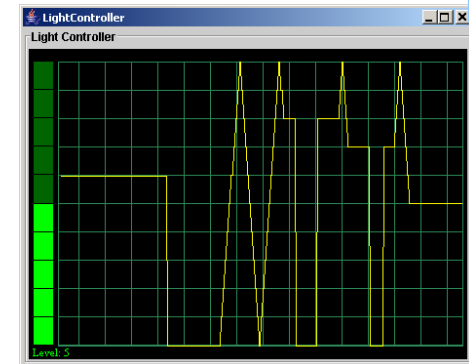
starthold!

endhold!



Control Program

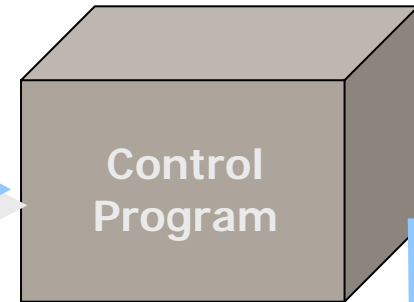
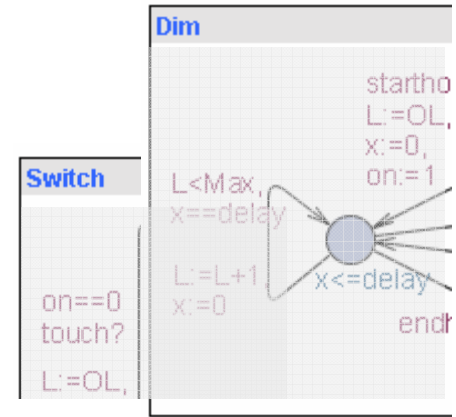
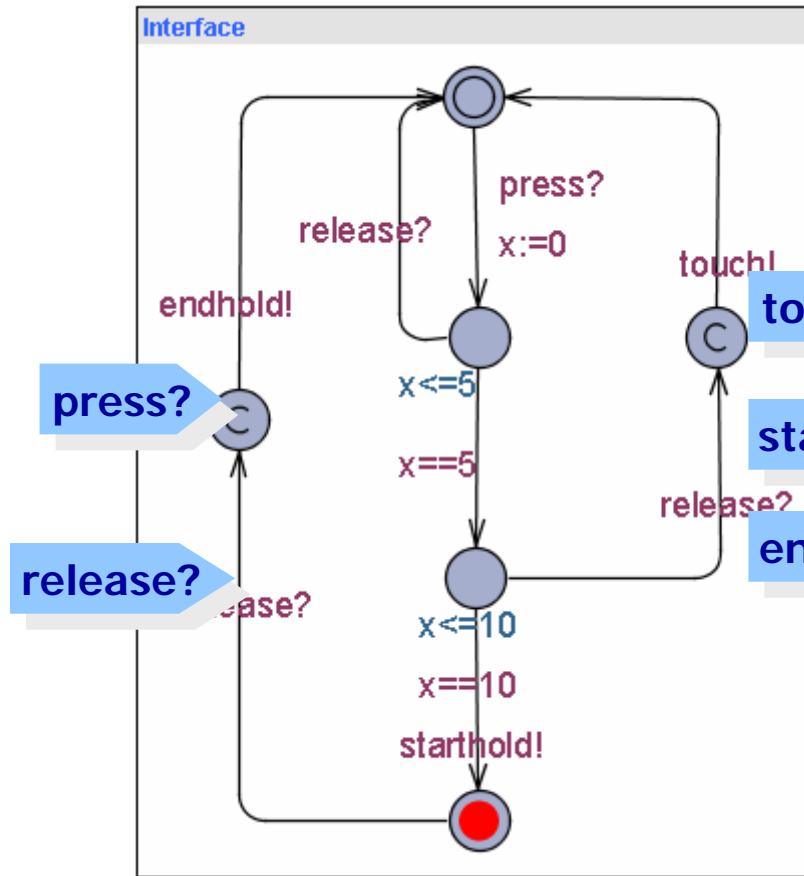
L++/L--/L:=0



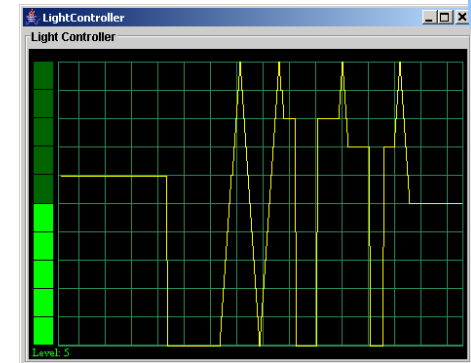
Light Control Interface



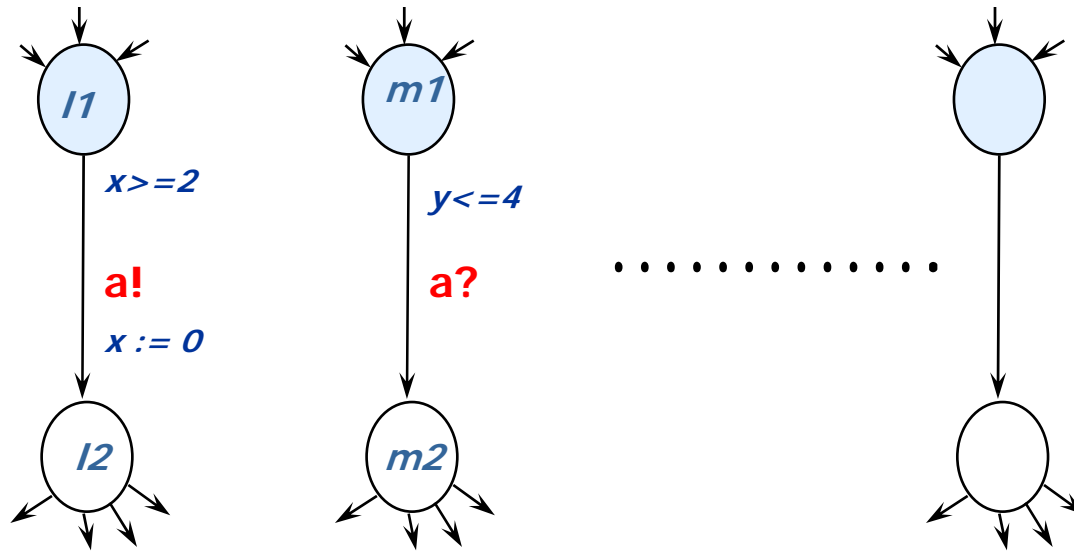
User



L++/L--/L:=0

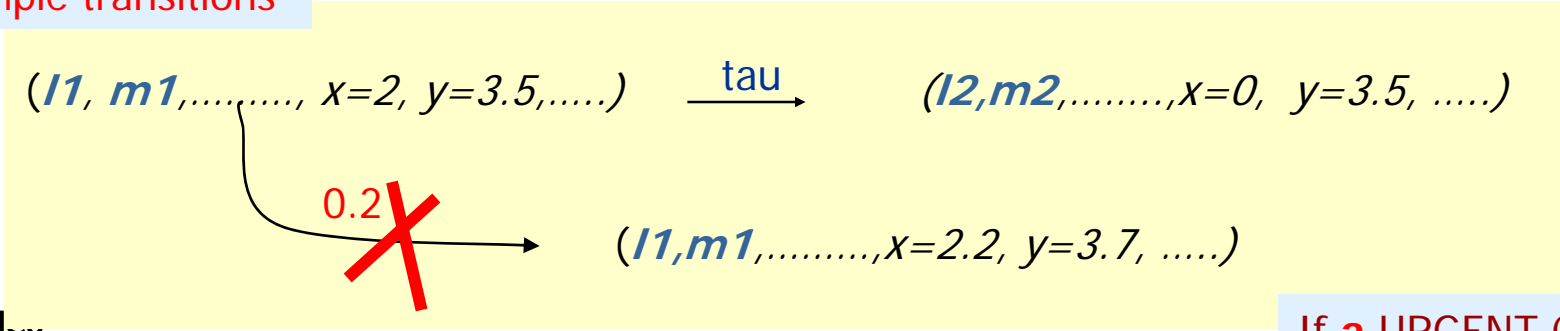


Networks of Timed Automata (a'la CCS)



Two-way synchronization on *complementary* actions.
Closed Systems!

Example transitions



If **a** URGENT CHANNEL

Network Semantics

$$T_1 \parallel_X T_2 = (S_1 \times S_2, \rightarrow, s_0^1 \parallel_X s_0^2) \quad \text{where}$$

$$\frac{S_1 \xrightarrow{\mu} S_1'}{S_1 \parallel_X S_2 \xrightarrow{\mu} S_1' \parallel_X S_2}$$

$$\frac{S_2 \xrightarrow{\mu} S_2'}{S_1 \parallel_X S_2 \xrightarrow{\mu} S_1 \parallel_X S_2'}$$

$$\frac{S_1 \xrightarrow{a!} S_1' \quad S_2 \xrightarrow{a?} S_2'}{S_1 \parallel_X S_2 \xrightarrow{\tau} S_1' \parallel_X S_2'}$$

$$\frac{S_1 \xrightarrow{e(d)} S_1' \quad S_2 \xrightarrow{e(d)} S_2'}{S_1 \parallel_X S_2 \xrightarrow{e(d)} S_1' \parallel_X S_2'}$$

Network Semantics

(URGENT synchronization)

+ Urgent synchronization

$$T_1 \parallel_X T_2 = (S_1 \times S_2, \rightarrow, s_0^1 \parallel_X s_0^2) \quad \text{where}$$

$$\frac{S_1 \xrightarrow{\mu} S_1'}{S_1 \parallel_X S_2 \xrightarrow{\mu} S_1' \parallel_X S_2}$$

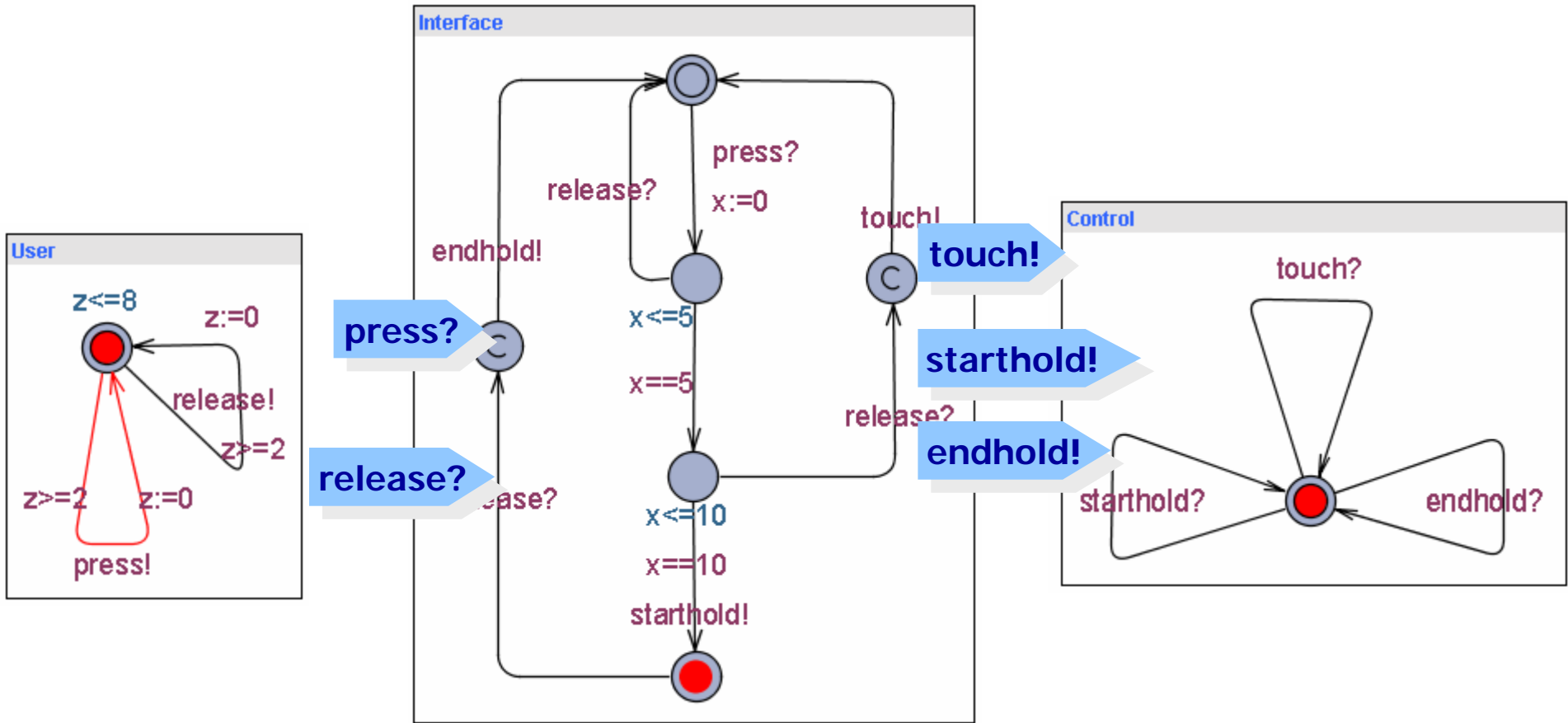
$$\frac{S_2 \xrightarrow{\mu} S_2'}{S_1 \parallel_X S_2 \xrightarrow{\mu} S_1 \parallel_X S_2'}$$

$$\frac{S_1 \xrightarrow{a!} S_1' \quad S_2 \xrightarrow{a?} S_2'}{S_1 \parallel_X S_2 \xrightarrow{\tau} S_1' \parallel_X S_2'}$$

$$\frac{S_1 \xrightarrow{e(d)} S_1' \quad S_2 \xrightarrow{e(d)} S_2'}{S_1 \parallel_X S_2 \xrightarrow{e(d)} S_1' \parallel_X S_2'}$$

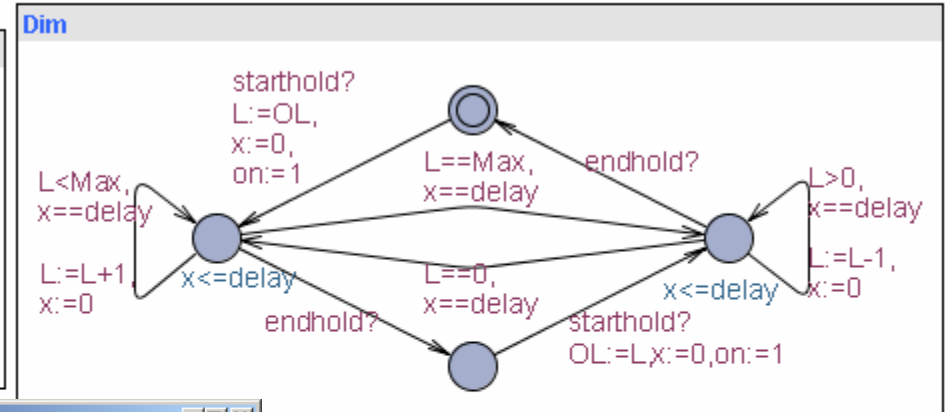
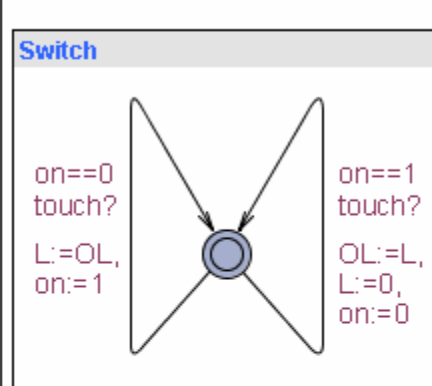
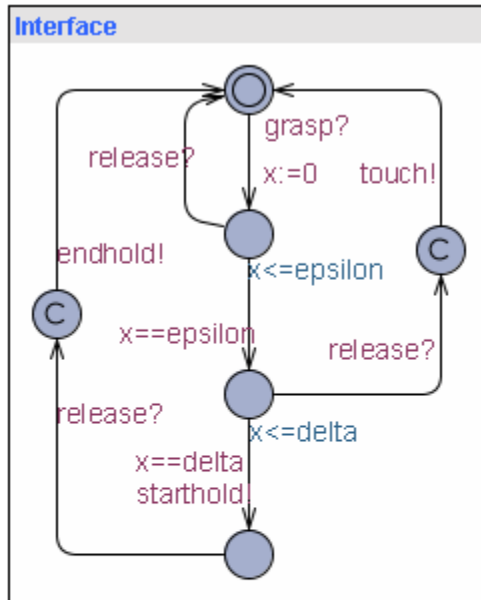
$$\forall d' < d, \forall u \in \text{UAct}: \neg (S_1 \xrightarrow{e(d') u?} \rightarrow \wedge S_2 \xrightarrow{e(d') u!} \rightarrow)$$

Light Control Network

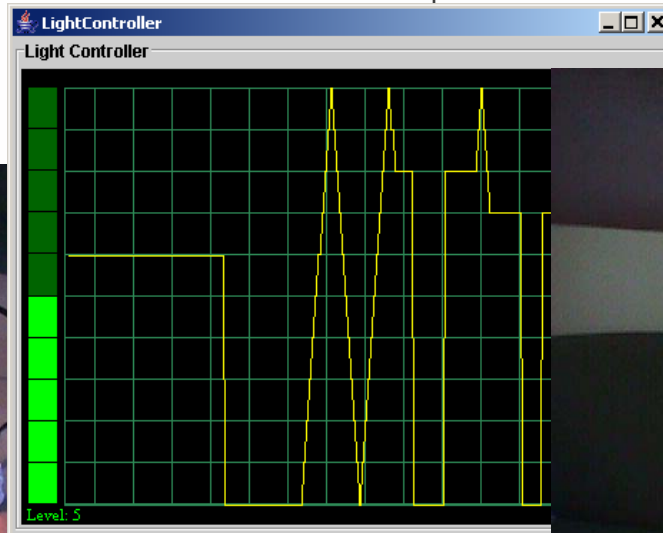
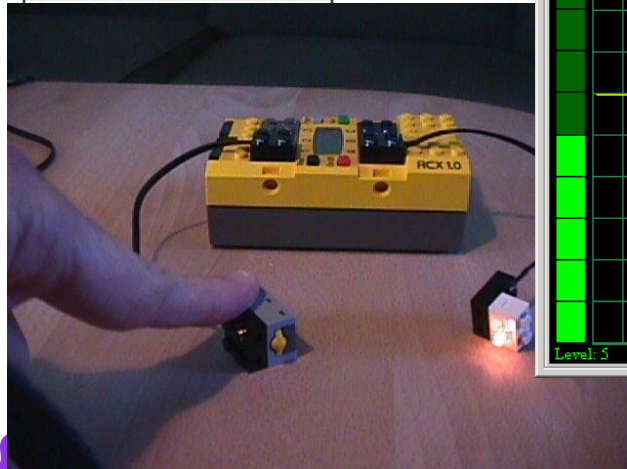


Validation

Light Controller



User





Druzba:

The Shower Problem



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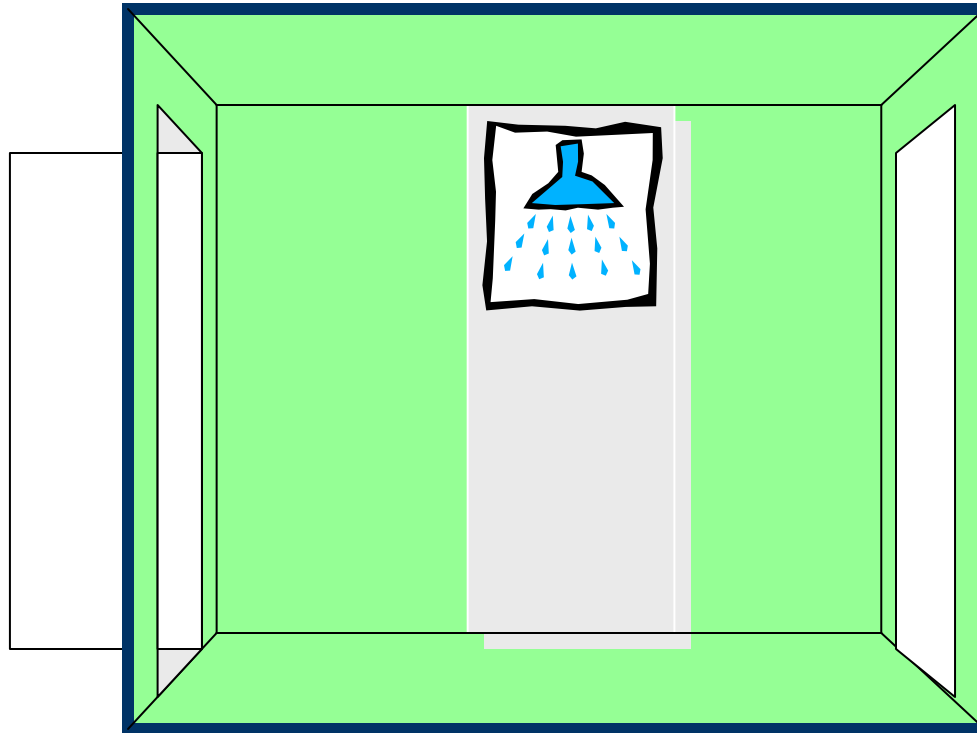


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The Druzba MUTEX Problem

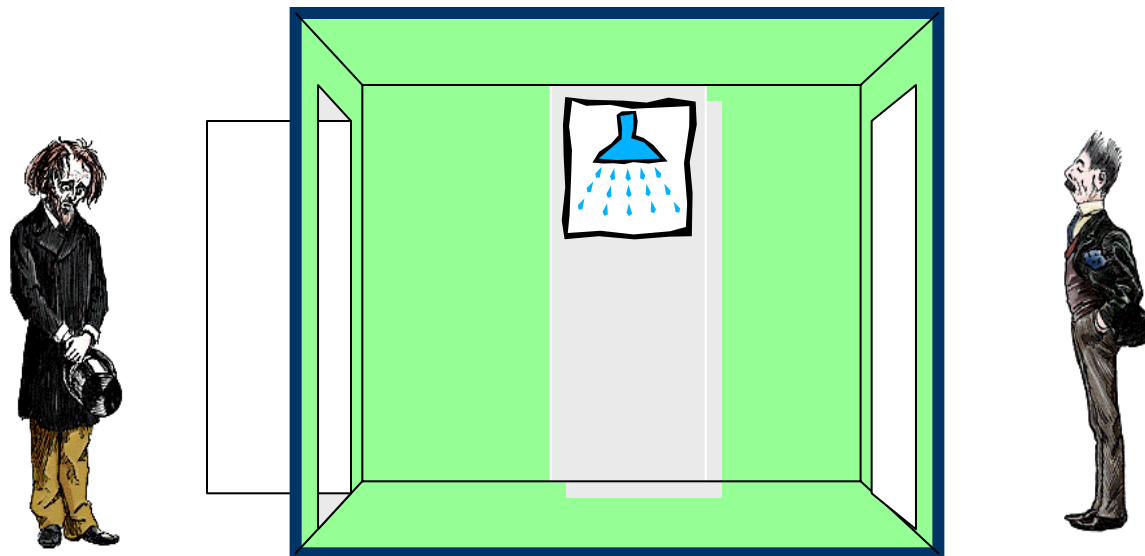
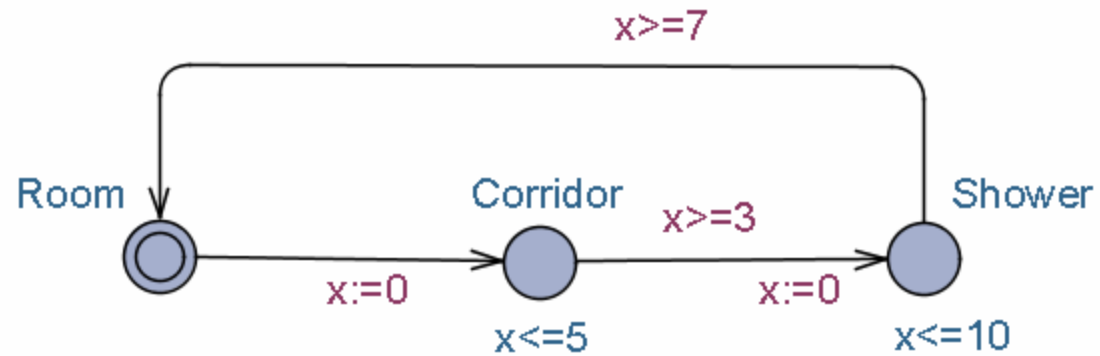


Kim



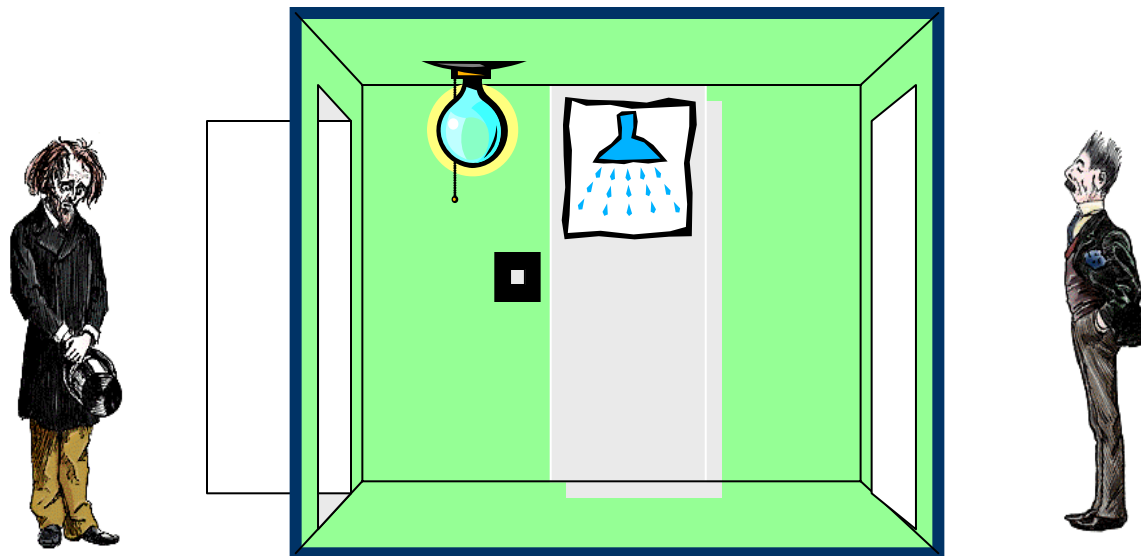
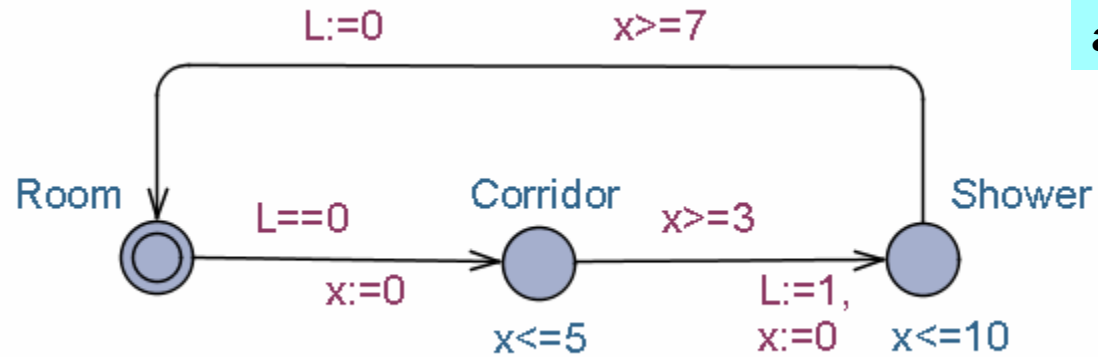
Gerd

The Druzba MUTEX Problem



The Druzba MUTEX Problem

Using the light as semaphore



Overview of the UPPAAL Toolkit



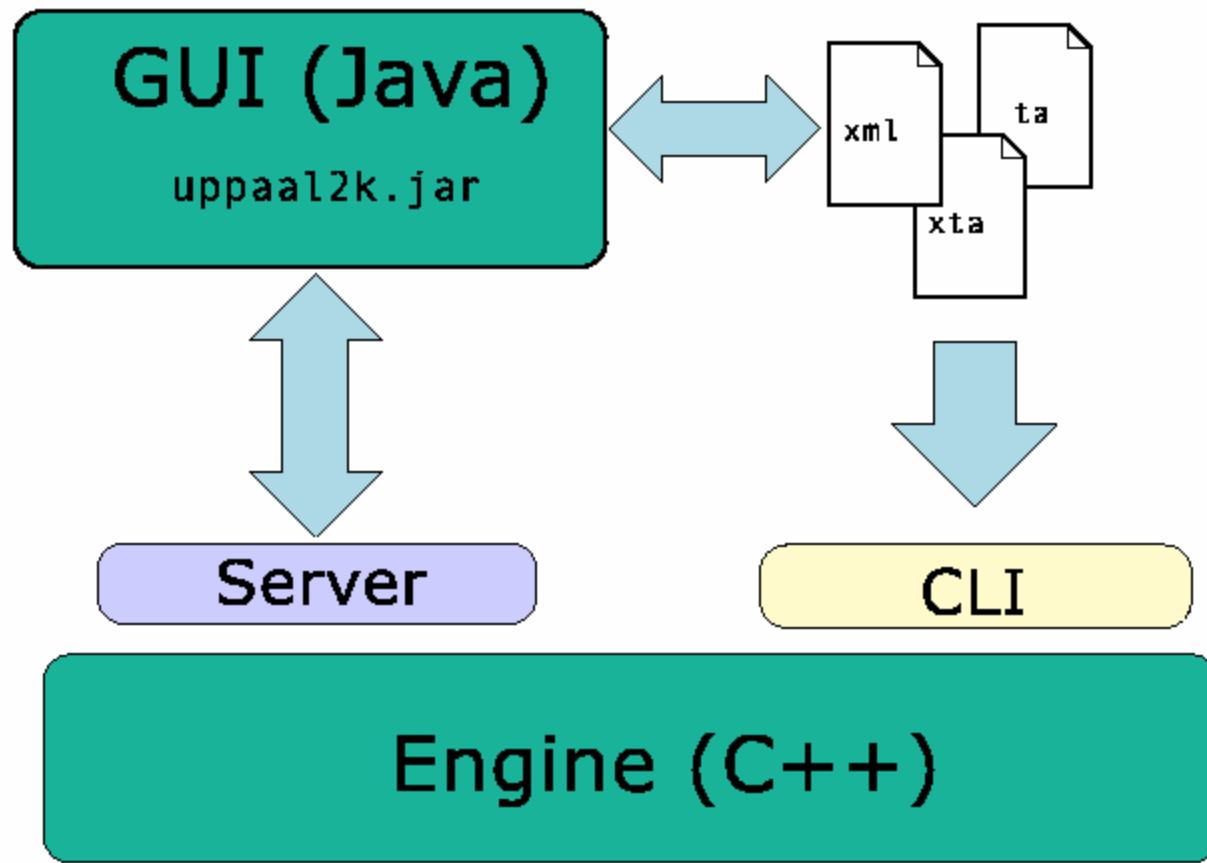
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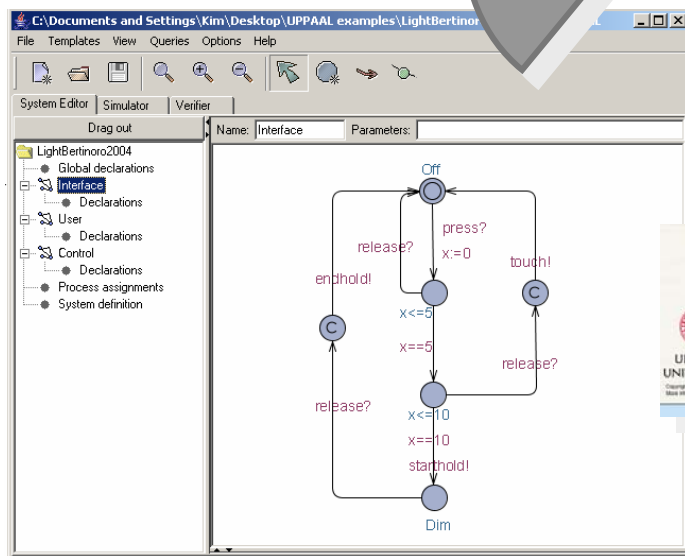
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UPPAAL's architecture

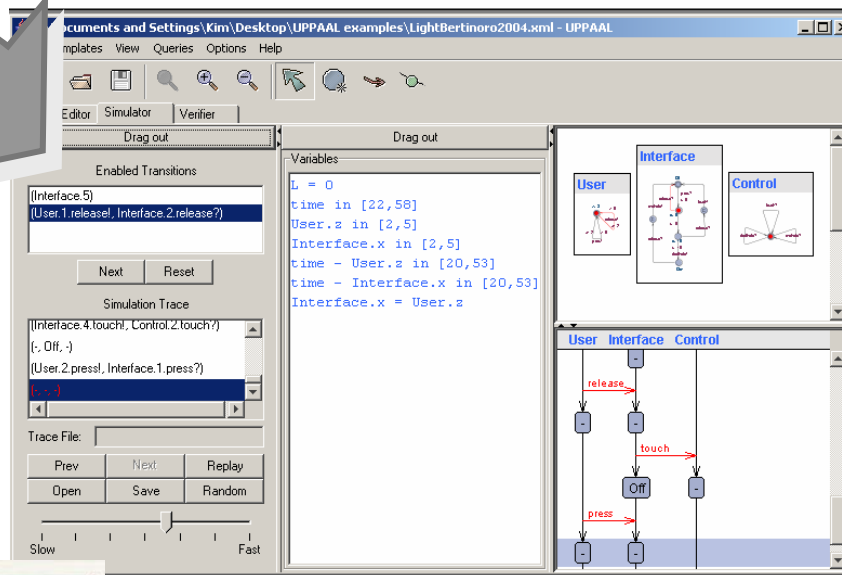


Linux, Windows, Solaris, MacOS

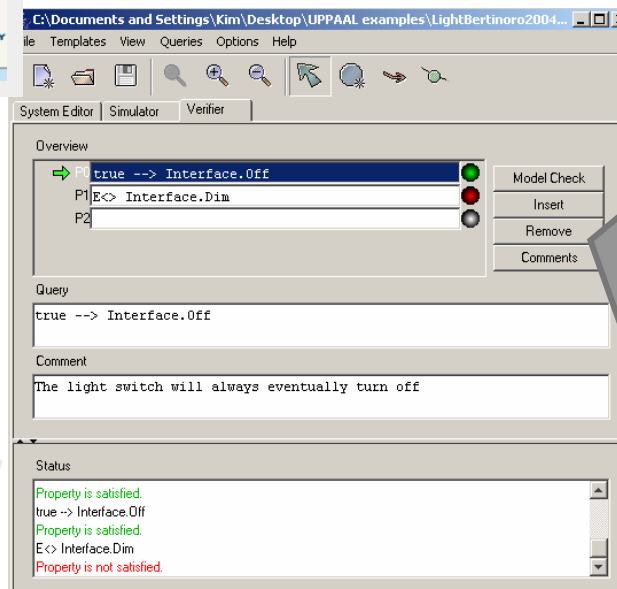
GUI



Editor

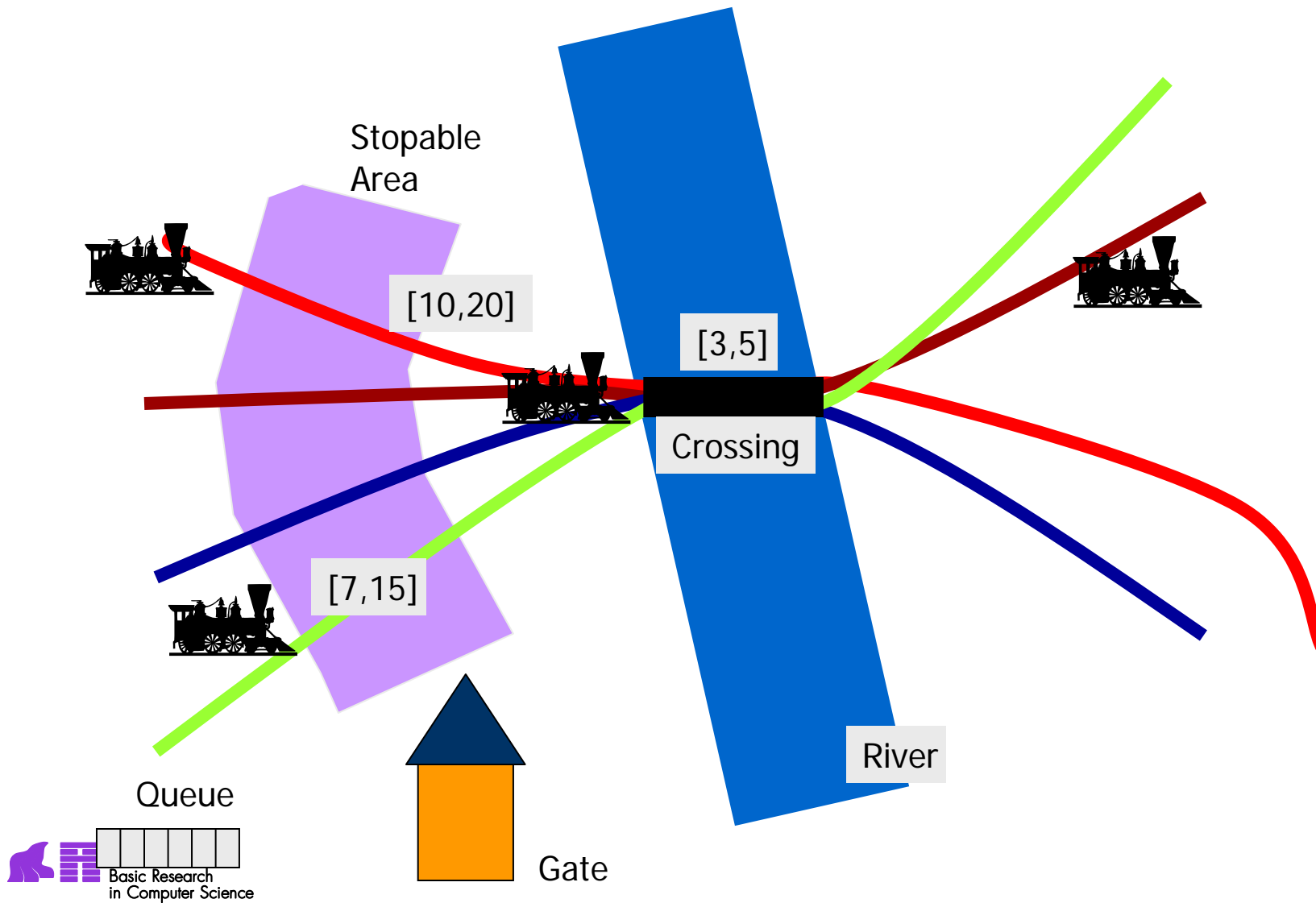


Simulator



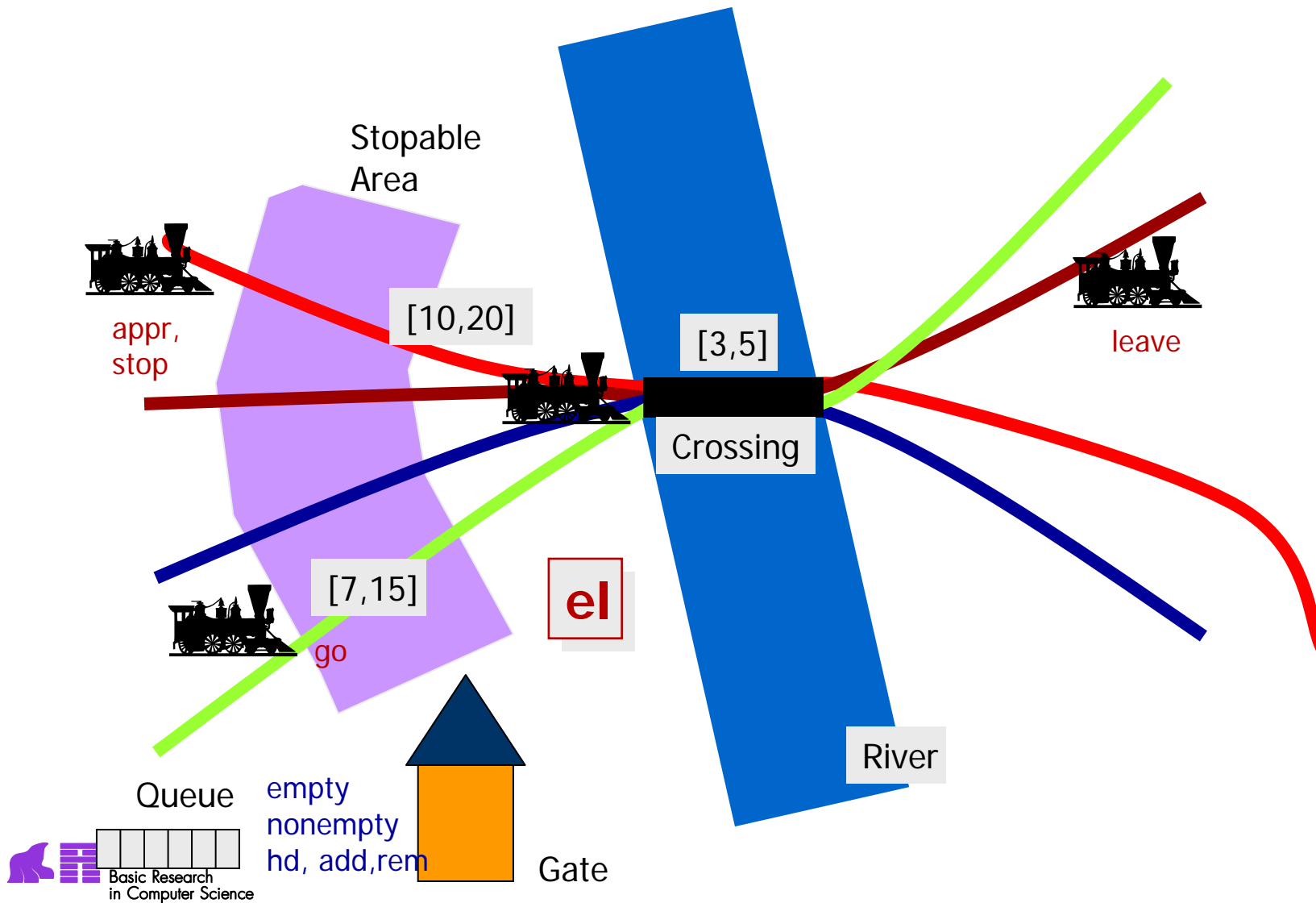
Verifier

Train Crossing



Train Crossing

Communication via channels and shared variable.



Timed Automata in UPPAAL



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Declarations

<ul style="list-style-type: none"> train-gate <ul style="list-style-type: none"> Global declarations 	<pre> /* * For more details about this example, see * "Automatic Verification of Real-Time Communicating Systems by Constraint Solving", * by Wang Yi, Paul Pettersson and Mats Daniels. In Proceedings of the 7th International * Conference on Formal Description Techniques, pages 223-238, North-Holland. 1994. */ const N 5; // # trains + 1 int[0,N] e1; chan appr, stop, go, leave; chan empty, notempty, hd, add, rem; </pre>
<ul style="list-style-type: none"> train-gate <ul style="list-style-type: none"> Declarations 	<pre> clock x; </pre>
<ul style="list-style-type: none"> train-gate <ul style="list-style-type: none"> Declarations 	<pre> int[0,N] list[N], len, i; </pre>
<ul style="list-style-type: none"> Process assignments 	<pre> Train1:=Train(e1, 1); Train2:=Train(e1, 2); Train3:=Train(e1, 3); Train4:=Train(e1, 4); </pre>
<ul style="list-style-type: none"> System definition 	<pre> system Train1, Train2, Train3, Train4, Gate, Queue; </pre>

- Constants
- Bounded integers
- Channels
- Clocks
- Arrays

- Templates
- Processes
- Systems



Declarations in UPPAAL

- The syntax used for declarations in UPPAAL is similar to the syntax used in the C programming language.

- **Clocks:**

- Syntax:

```
clock x1, ..., xn ;
```

- Example:

```
clock x, y;
```

Declares two clocks: x and y.

Declarations in UPPAAL (cont.)

■ Data variables

- Syntax:

```
- int n1, ... ;
- int[l,u] n1, ... ;
- int n1[m], ... ;
```

Integer with “default” domain.

Integer with domain “l” to “u”.

Integer array w. elements
n1[0] to n1[m-1].

- Example:

```
- int a, b;
- int[0,1] a, b[5][6];
```

Declarations in UPPAAL (cont.)

- **Actions** (or channels):

- Syntax:

```

- chan a, ... ;
- urgent chan b, ... ;
  
```

Ordinary channels.

Urgent actions (see later)

- Example:

- `chan a, b;`

- `urgent chan c;`

Declarations UPPAAL (cont.)

■ Constants

- Syntax:

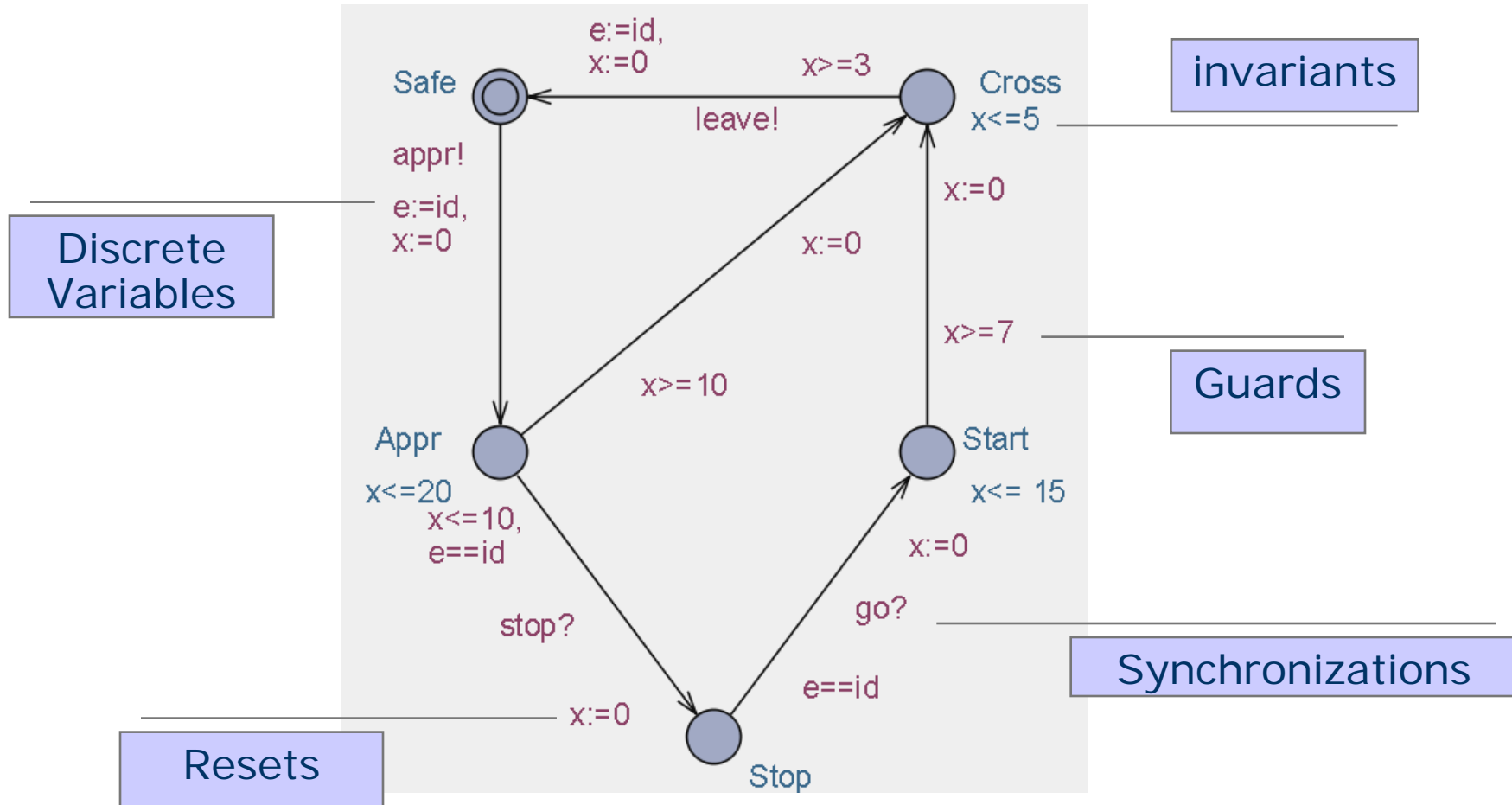
```
- const int c1 = n1;
```

- Example:

```
- const int[0,1] YES = 1;
```

```
- const bool NO = false;
```

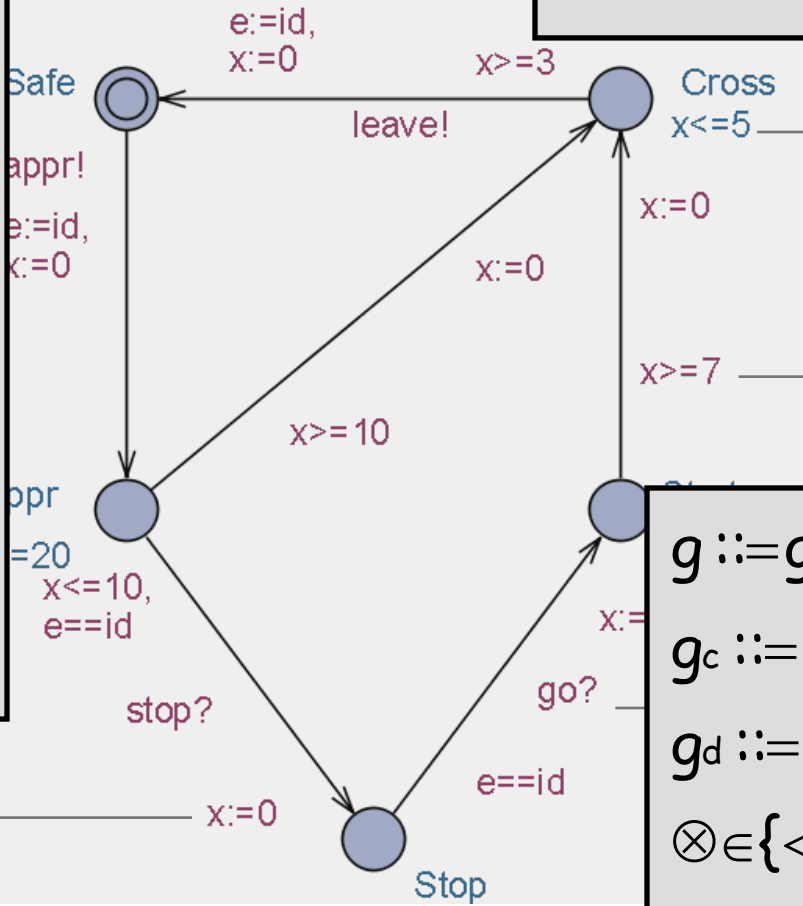
Timed Automata in UPPAAL



Timed Automata in UPPAAL

$i ::= \text{Expr}$
 $\text{Expr} ::= i \mid i[\text{Expr}] \mid$
 $n \mid -\text{Expr} \mid$
 $\text{Expr} + \text{Expr} \mid$
 $\text{Expr} - \text{Expr} \mid$
 $\text{Expr} * \text{Expr} \mid$
 $\text{Expr} / \text{Expr} \mid$
 $(g_d ? \text{Expr} : \text{Expr})$

$\text{inv} ::= x < \text{Expr} \mid x \leq \text{Expr} \mid \text{inv}, \text{inv}$



invariants

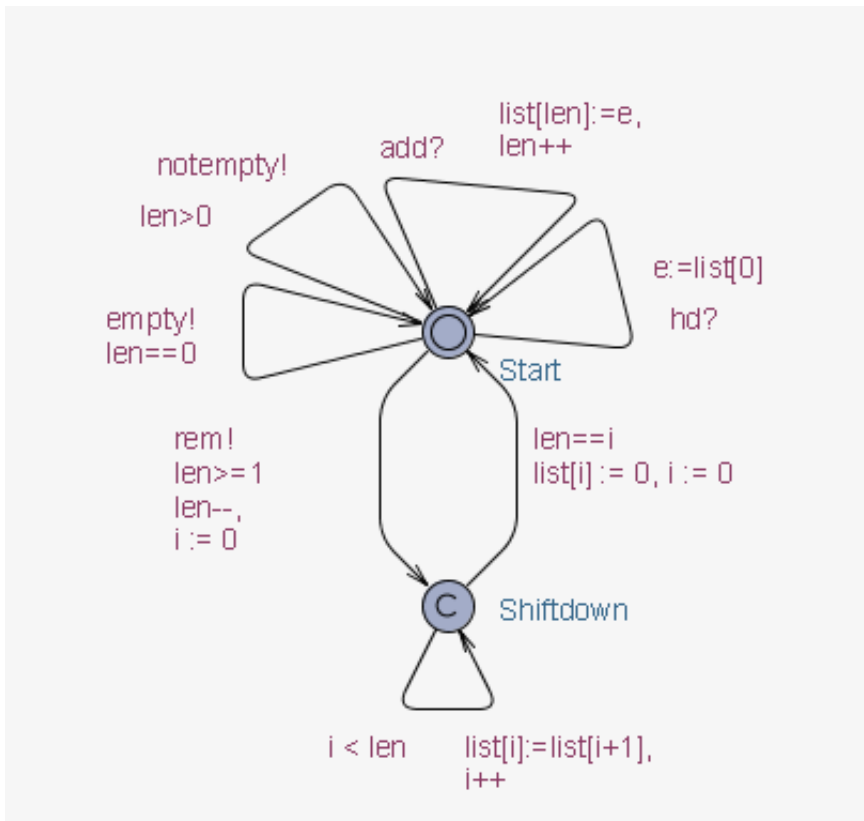
Guards

Resets

$x := \text{Expr}$

$g ::= g_c \mid g_d \mid g, g$
 $g_c ::= x \otimes \text{Expr} \mid x \otimes y + \text{Expr}$
 $g_d ::= \text{Expr op Expr}$
 $\otimes \in \{<, \leq, =, \geq, >\}$
 $\text{op} \in \{<, \leq, =, \geq, >, !=\}$

Expressions



used in

- guards,
- invariants,
- assignments,
- synchronizations
- properties,

Expressions

```

Expression
 ::= ID
 | NAT
 | Expression '[' Expression ']'
 | '(' Expression ')'
 | Expression '++' | '++' Expression
 | Expression '--' | '--' Expression
 | Expression AssignOp Expression
 | UnaryOp Expression
 | Expression BinOp Expression
 | Expression '?' Expression ':' Expression
 | ID '.' ID
  
```

Operators

Unary

'-' | '!' | 'not'

Binary

'<' | '<=' | '==' | '!=' | '>=' | '>'
 '+' | '-' | '*' | '/' | '%' | '&'
 '|' | '^' | '<<' | '>>' | '&&' | '||'
 'and' | 'or' | 'imply'

Assignment

':=' | '+=' | '-=' | '*=' | '/=' | '%='
 '|=' | '&=' | '^=' | '<<=' | '>>='

Guards, Invariants, Assignments

Guards:

- It is side-effect free, type correct, and evaluates to boolean
- Only clock variables, integer variables, constants are referenced (or arrays of such)
- **Clocks and differences are only compared to integer expressions**
- Guards over clocks are essentially conjunctions (I.e. disjunctions are only allowed over integer conditions)

Assignments

- It has a side effect and is type correct
- Only clock variable, integer variables and constants are referenced (or arrays of such)
- **Only integer are assigned to clocks**

Invariants

- It forms conjunctions of conditions of the form $x < e$ or $x \leq e$ where x is a clock reference and e evaluates to an integer

Synchronization

Binary Synchronization

- Declared like:
`chan a, b, c[3];`
- If a is channel then:
 - a! = Emmission
 - a? = Reception
- **Two edges** in different processes can synchronize if one is emitting and the other is receiving on the same channel.

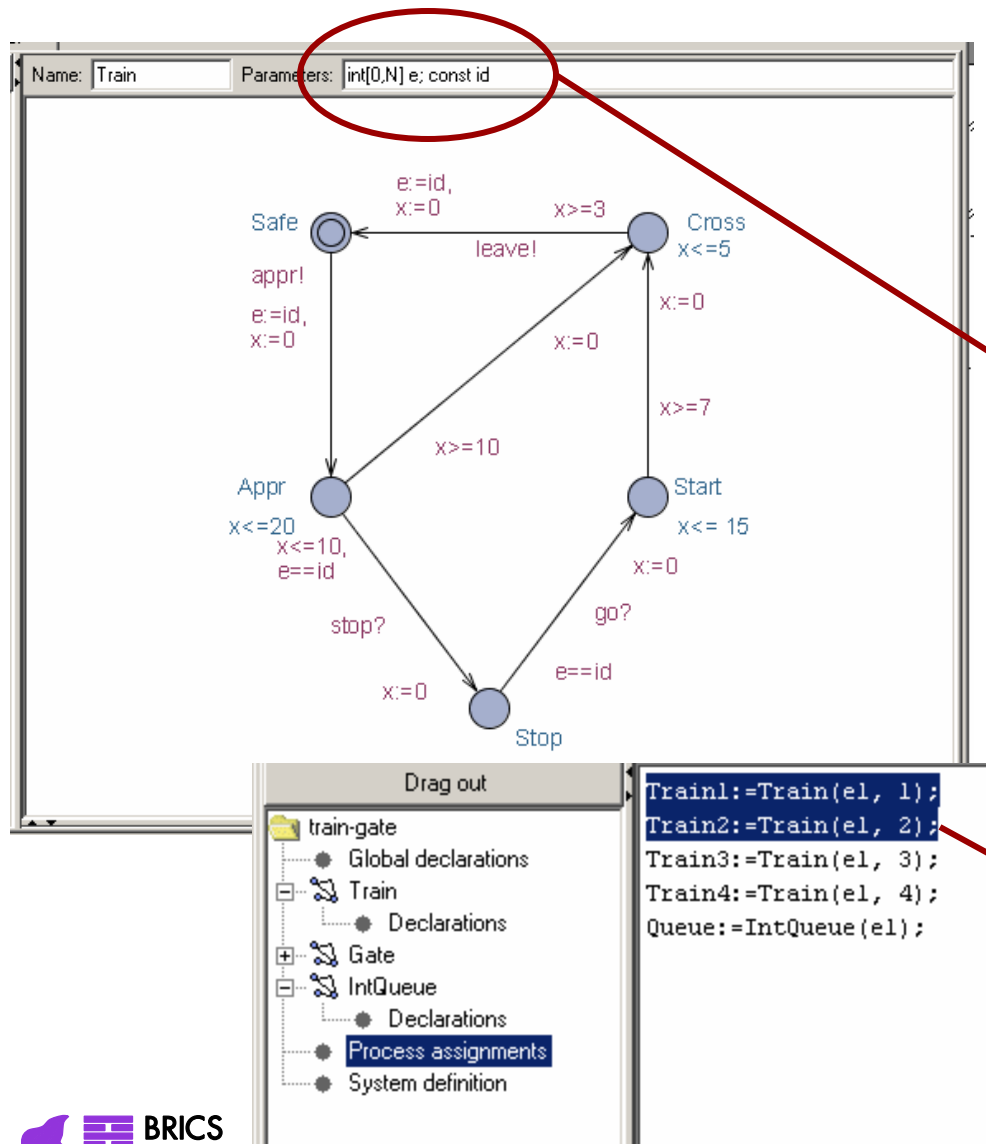
Broadcast Synchronization

- Declared like
`broadcast chan a, b, c[2];`
- If a is a broadcast channel:
 - a! = Emmission of broadcast
 - a? = Reception of broadcast
- **A set of edges** in different processes can synchronize if one is emitting and the others are receiving on the same b.c. channle. A process can always emit.
 Receivers **MUST** synchronize if they can.
 No blocking.

More on Types

- Multi dimensional arrays
 - e.g. `int b[4][2];`
- Array initialiser:
 - e.g. `int b[4] := { 1, 2, 3, 4 };`
- Arrays of channels, clocks, constants.
 - e.g.
 - `chan a[3];`
 - `clock c[3];`
 - `const k[3] { 1, 2, 3 };`
- Broadcast channels.
 - e.g. `broadcast chan a;`

Templates



- Templates may be **parameterised**:

- int v; const min;
const max

- int[0,N] e; const id

- Templates are **instantiated** to form processes:

- P := A(i, 1, 5);

- Q := A(j, 0, 4);

- Train1 := Train(e1, 1);

- Train2 := Train(e1, 2);

Extensions

Select statement

- models a non-deterministic choice
- `x : int[0,42]`

Types

- Record types
- Type declarations
- Meta variables:
not stored with state
`meta int x;`

Forall / Exists expressions

- `forall (x:int[0,42]) expr`
true if `expr` is true for *all* values in `[0,42]` of `x`
- `exists (x:int[0,4]) expr`
true if `expr` is true for *some* values in `[0,42]` of `x`

Example:

```
forall
(x:int[0,4])array[x];
```

Urgency & Commitment

Urgent Channels

- No delay if the synchronization edges can be taken !
- No clock guard allowed.
- Guards on data-variables.
- Declarations:
urgent chan a, b,
c[3];

Urgent Locations

- No delay – time is freezed!
- May reduce number of clocks!

Committed Locations

- No delay.
- Next transition MUST involve edge in one of the processes in committed location
- May reduce considerably state space

Queries : Specification Language



BRICS

Basic Research
in Computer Science



CENTER FOR INDLEJREDE SOFTWARE SYSTEMER

Logical Specifications

■ Validation Properties

- Possibly: $E \leftrightarrow P$

■ Safety Properties

- Invariant: $A[] P$
- Pos. Inv.: $E[] P$

■ Liveness Properties

- Eventually: $A \leftrightarrow P$
- Leadsto: $P \rightarrow Q$

■ Bounded Liveness

- Leads to within: $P \rightarrow_{\leq t} Q$

The expressions P and Q must be type safe, side effect free, and evaluate to a boolean.

Only references to integer variables, constants, clocks, **and locations** are allowed (and arrays of these).

Logical Specifications

■ Validation Properties

- Possibly: $E \langle \rangle P$

■ Safety Properties

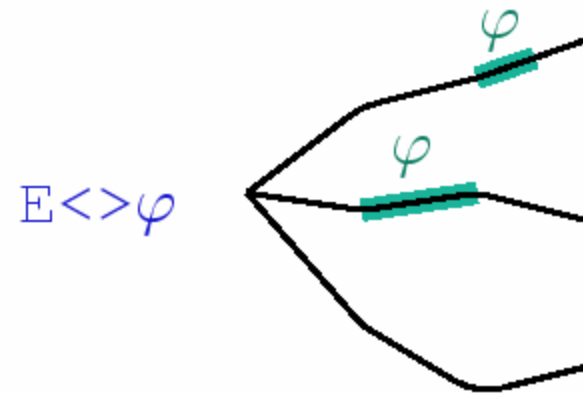
- Invariant: $A [] P$
- Pos. Inv.: $E [] P$

■ Liveness Properties

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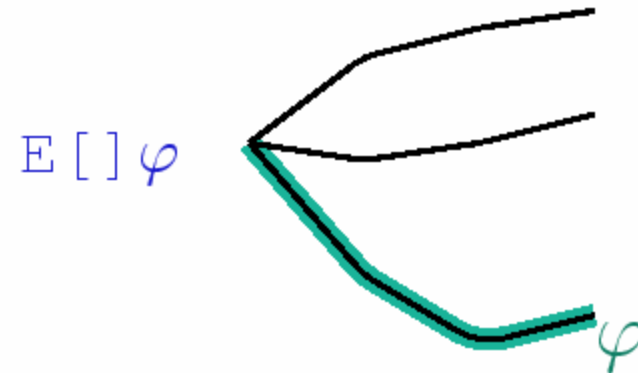
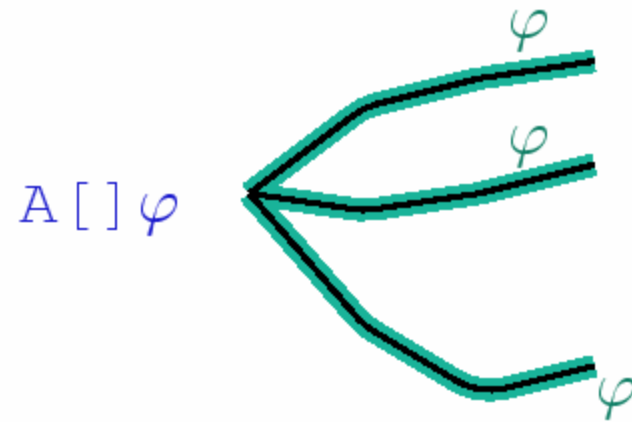
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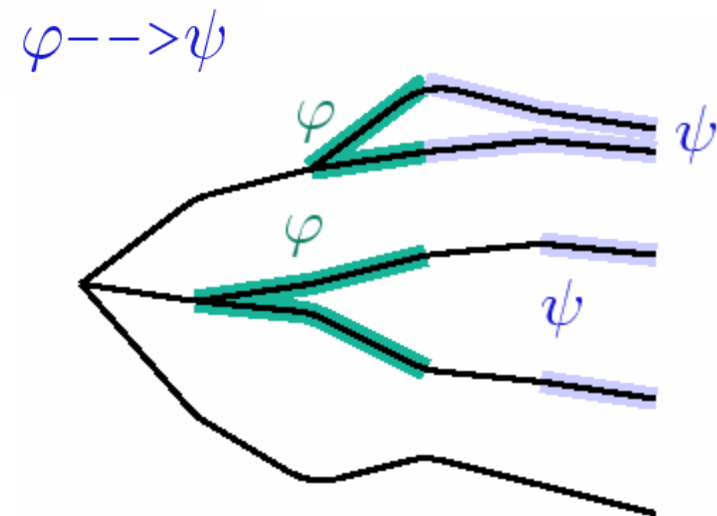
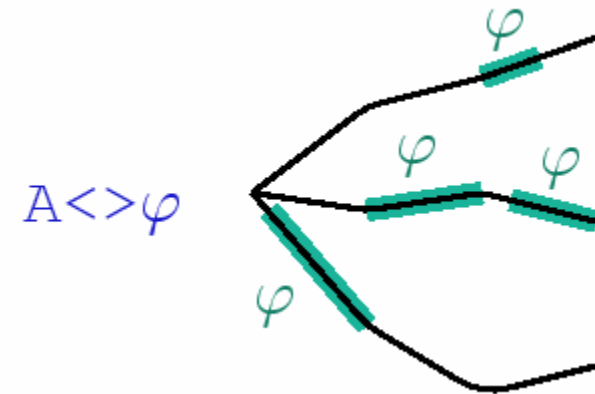
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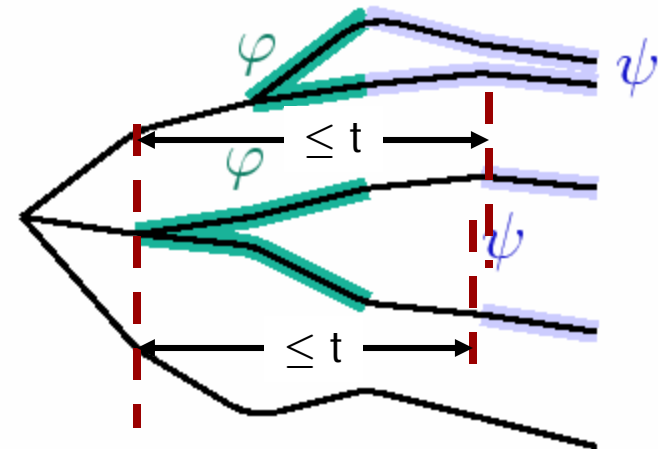
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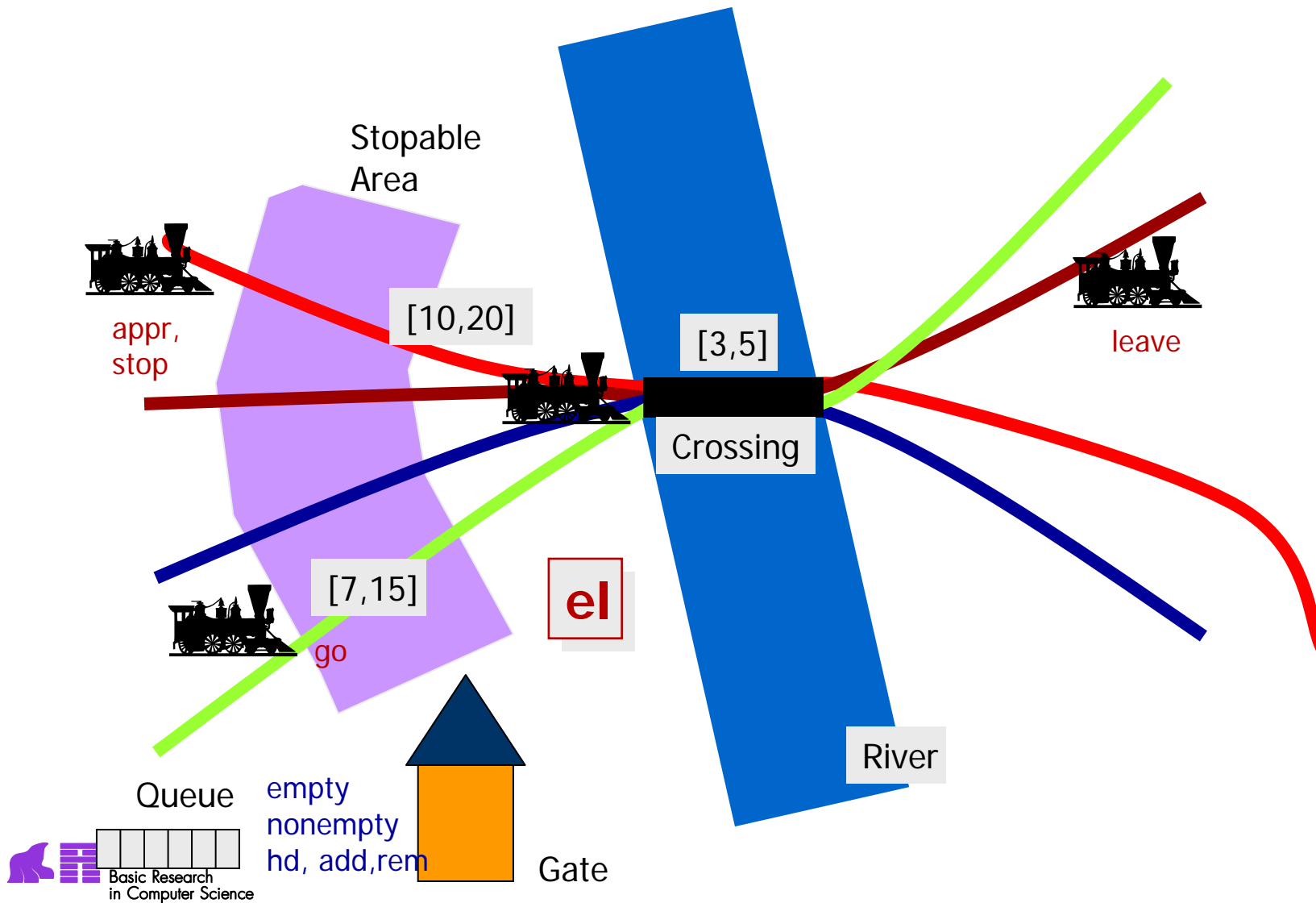
- Liveness Properties
 - Eventually: $A \leftrightarrow P$
 - Leadsto: $P \rightarrow Q$

- Bounded Liveness
 - Leads to within: $P \rightarrow_{\leq t} Q$



Train Crossing

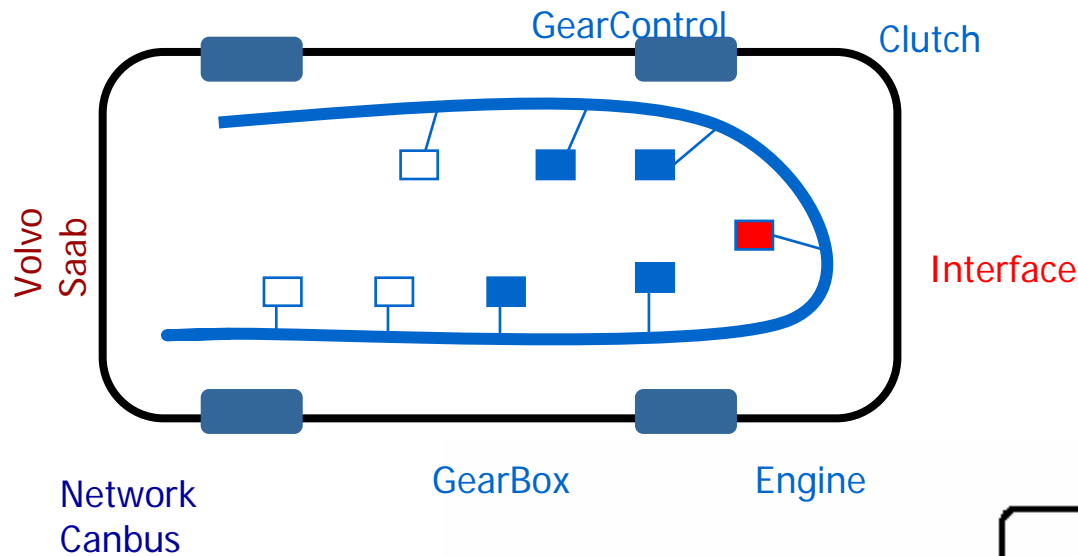
Communication via channels and shared variable.



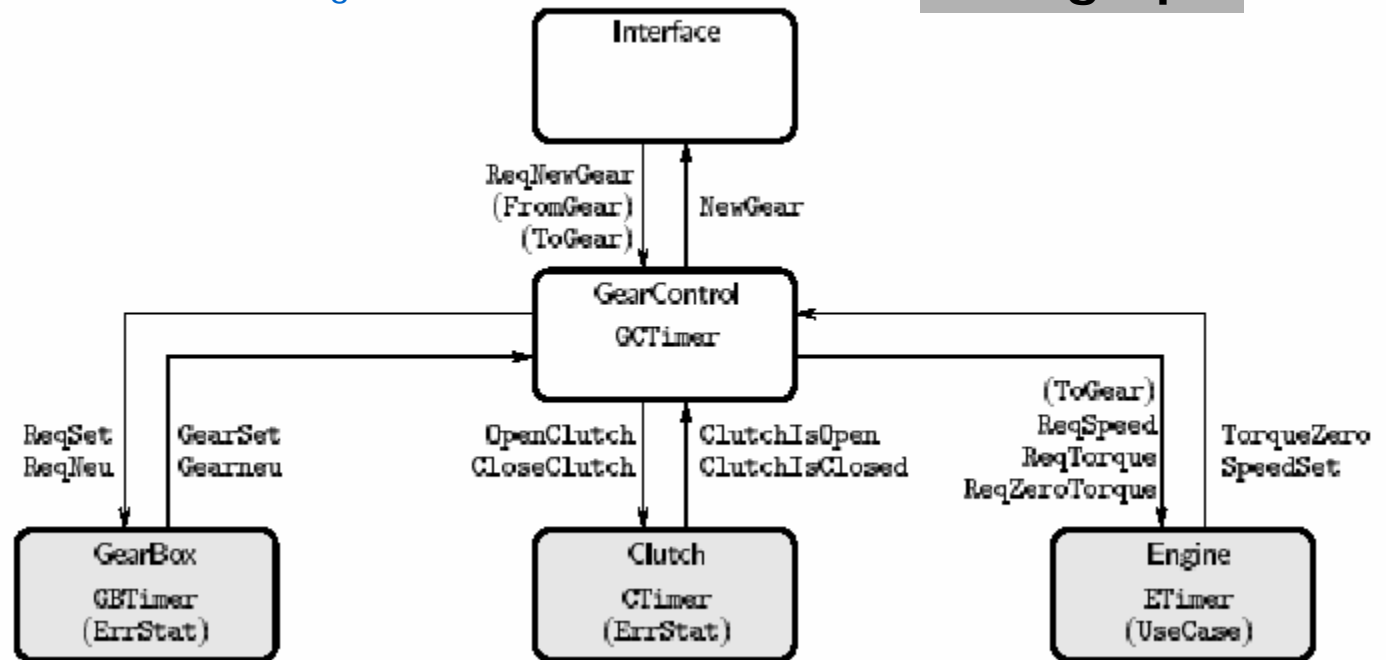
Gear Controller

with MECEL AB

Lindahl, Pettersson, Yi 1998

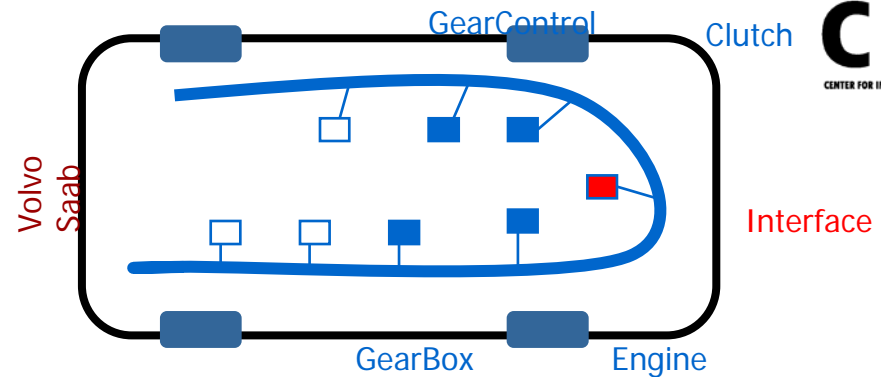


Flowgraph



Gear Controller

with MECEL AB



Requirements

$$\text{GearControl@Initiate} \rightsquigarrow_{\leq 1500} ((\text{ErrStat} = 0) \Rightarrow \text{GearControl@GearChanged}) \quad (1)$$

$$\begin{aligned} \text{GearControl@Initiate} \rightsquigarrow_{\leq 1000} \\ ((\text{ErrStat} = 0 \wedge \text{UseCase} = 0) \Rightarrow \text{GearControl@GearChanged}) \end{aligned} \quad (2)$$

$$\text{Clutch@ErrorClose} \rightsquigarrow_{\leq 200} \text{GearControl@CCloseError} \quad (3)$$

$$\text{Clutch@ErrorOpen} \rightsquigarrow_{\leq 200} \text{GearControl@COpenError} \quad (4)$$

$$\text{GearBox@ErrorIdle} \rightsquigarrow_{\leq 350} \text{GearControl@GSetError} \quad (5)$$

$$\text{GearBox@ErrorNeu} \rightsquigarrow_{\leq 200} \text{GearControl@GNeuError} \quad (6)$$

$$\text{Inv} (\text{GearControl@CCloseError} \Rightarrow \text{Clutch@ErrorClose}) \quad (7)$$

$$\text{Inv} (\text{GearControl@COpenError} \Rightarrow \text{Clutch@ErrorOpen}) \quad (8)$$

$$\text{Inv} (\text{GearControl@GSetError} \Rightarrow \text{GearBox@ErrorIdle}) \quad (9)$$

$$\text{Inv} (\text{GearControl@GNeuError} \Rightarrow \text{GearBox@ErrorNeu}) \quad (10)$$

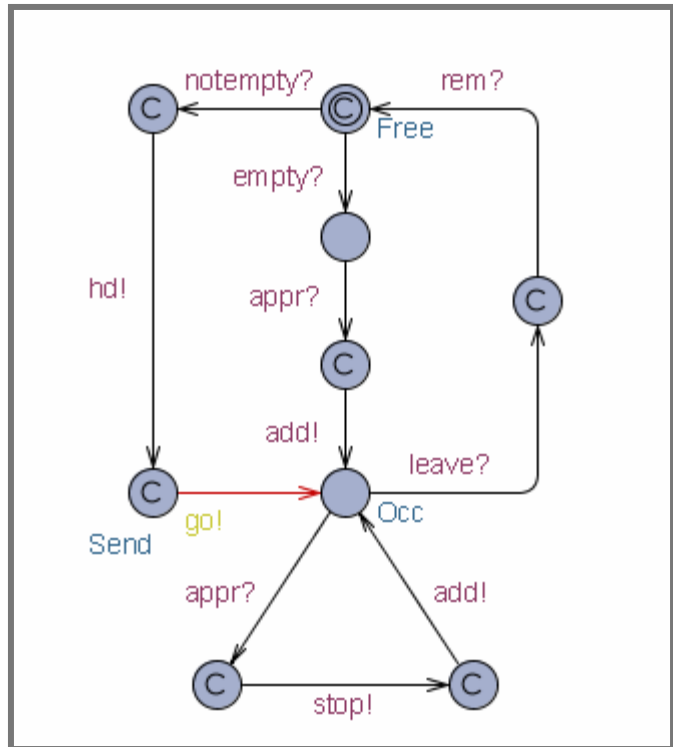
$$\text{Inv} (\text{Engine@ErrorSpeed} \Rightarrow \text{ErrStat} \neq 0) \quad (11)$$

$$\text{Inv} (\text{Engine@Torque} \Rightarrow \text{Clutch@Closed}) \quad (12)$$

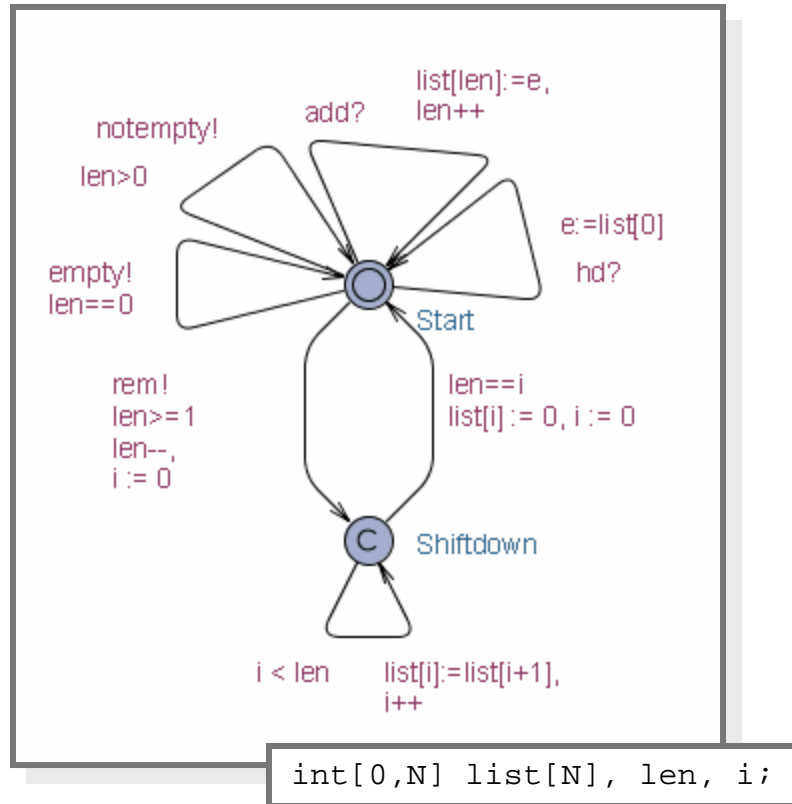
$$\bigwedge_{i \in \{R, N, 1, \dots, 5\}} \text{Poss} (\text{Gear@Gear}_i) \quad (13)$$

$$\bigwedge_{i \in \{R, 1, \dots, 5\}} \text{Inv} ((\text{GearControl@Gear} \wedge \text{Gear@Gear}_i) \Rightarrow \text{Engine@Torque}) \quad (14)$$

UPPAAL 3.4

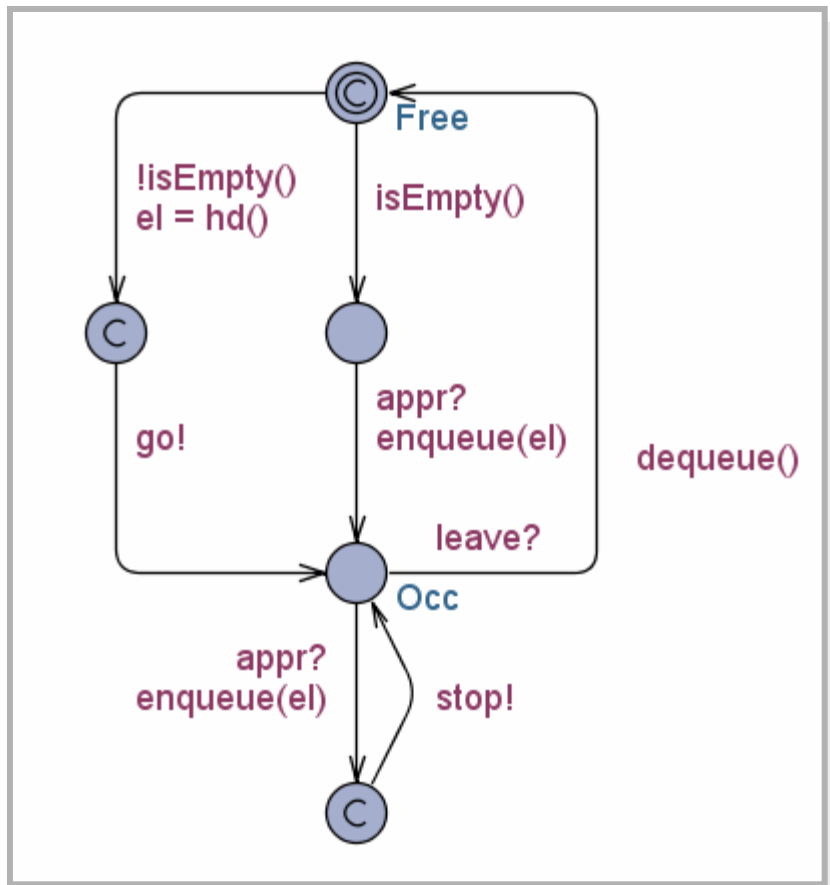


Gate Template



IntQueue

UPPAAL 3.6 (3.5) with C-Code



Gate Template

```

int[0,N] list[N], len;

void enqueue(int[0,N] element)
{
    list[len++] = element;
}

void dequeue()
{
    int i = 0;
    len -= 1;
    while (i < len)
    {
        list[i] = list[i + 1];
        i++;
    }
    list[i] = 0;
    i = 0;
}

bool isEmpty()
{
    return len == 0;
}

int[0,N] hd()
{
    return list[0];
}

```

Gate Declaration

Case-Studies: Controllers

- Gearbox Controller [TACAS'98]
- Bang & Olufsen Power Controller [RTPS'99, FTRTFT'2k]
- SIDMAR Steel Production Plant [RTCSA'99, DSVV'2k]
- Real-Time RCX Control-Programs [ECRTS'2k]
- Experimental Batch Plant (2000)
- RCX Production Cell (2000)
- Terma, Verification of Memory Management for Radar (2001)
- Scheduling Lacquer Production (2005)
- Memory Arbiter Synthesis and Verification for a Radar Memory Interface Card [NJC'05]

Case Studies: Protocols

- Philips Audio Protocol [HS'95, CAV'95, RTSS'95, CAV'96]
- Collision-Avoidance Protocol [SPIN'95]
- Bounded Retransmission Protocol [TACAS'97]
- Bang & Olufsen Audio/Video Protocol [RTSS'97]
- TDMA Protocol [PRFTS'97]
- Lip-Synchronization Protocol [FMICS'97]
- Multimedia Streams [DSVIS'98]
- ATM ABR Protocol [CAV'99]
- ABB Fieldbus Protocol [ECRTS'2k]
- IEEE 1394 Firewire Root Contention (2000)
- Distributed Agreement Protocol [Formats05]
- Leader Election for Mobile Ad Hoc Networks [Charme05]

UPPAAL

Home

Home | About | Documentation | Download | Examples | Bugs

UPPAAL is an integrated tool environment for modeling, validation and verification of real-time systems modeled as networks of timed automata, extended with data types (bounded integers, arrays, etc.).

The tool is developed in collaboration between the [Department of Information Technology](#) at Uppsala University, Sweden and the [Department of Computer Science](#) at Aalborg University in Denmark.

Download

The current official release is UPPAAL 3.4.11 (Jun 23, 2005). A release of UPPAAL **3.6 alpha 3** (dec 20, 2005) is also available. For more information about UPPAAL version 3.4, we refer to this [press release](#).

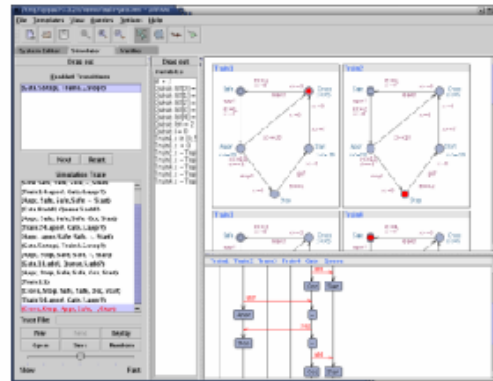


Figure 1: UPPAAL on screen.

License

The UPPAAL tool is **free** for non-profit applications. For information about commercial licenses, please email [sales\(at\)uppaal\(dot\)com](mailto:sales(at)uppaal(dot)com).

To find out more about UPPAAL, read this short [introduction](#). Further information may be found at this web site in the pages [About](#), [Documentation](#), [Download](#), and [Examples](#).

Mailing Lists

UPPAAL has an open [discussion forum](#) group at Yahoo!Groups intended for users of the tool. To join or post to the forum, please refer to the information at the [discussion forum](#) page. Bugs should be reported using the [bug tracking system](#). To email the development team directly, please use [uppaal\(at\)list\(dot\)it\(dot\)uu\(dot\)se](mailto:uppaal(at)list(dot)it(dot)uu(dot)se).



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